EE5323

VLSI Design I

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www.ece.umn.edu/users/kia

Slides Adapted from Prof. Chris Kim's F07 offering of the course

Course Information

- **Class webpage**
  - **http://www.ece.umn.edu/users/kia/Courses/EE5323**
- **Instructor: *Kia Bazargan***
  - **Office: EE/CSci 4-159, Email: kia@umn.edu**
  - **Ph: (612) 625 4588**
  - ***Office hrs*: MW 10-11, or by appointment**
- **TA: *Satish Sivaswamy***
  - **Office: VLSI Lab EE/CSci 1-200, Email: satish@umn.edu**
  - **Ph: (612) 626 7163**
  - ***Lab/office hrs:* TTh 11-12**
- **UNITE / WebVista webpage**
  - **www.myu.umn.edu**

UNITE

- **Class will be broadcast through the UNITE system**
- **Streaming video available**
  - **www.myu.umn.edu**
  - **Please attend class for more interaction**
- **To encourage your attendance, video will be available 10 days after the actual lecture (standard UNITE policy – no exceptions)**

Class Material

- **Textbook:**
  - **"Digital Integrated Circuits – A Design Perspective", 2nd ed, by J. Rabaey, A. Chandrakasan, B. Nikolic**
- **Writing on the board versus powerpoint**
- **Other references**
  - **I. E. Sutherland, R. F. Sproull, and D. F. Harris, Logical effort : Designing fast CMOS circuits, Morgan Kaufmann, San Francisco, CA, 1999.**
  - **Y. Taur, T. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, 2002.**

CAD Software

- **Cadence schematic and layout**
  - **Industry standard**
  - **Online tutorials**
  - **Companies prefer to hire students with design experience in Cadence environment (making you competitive for industry jobs is a big focus of this class)**
- **HSPICE for circuit simulation**
- **Cosmoscope for viewing results**
- **Technology file: 140nm**

- **VLSI lab: EE/CSci 1-200**
- **Off-campus students can use your company's tools**

Academic Integrity

- **Students caught engaging in an academically dishonest practice will receive a failing grade for the course.**

- **University policy on academic dishonesty will be followed strictly.**
  - **http://www1.umn.edu/oscai/**

Policies

- Homework must be received before class
  - 3 days of grace period to be used for all assignments (e.g., 1 day each for 3 assignments, or 3 days on one assignment)
  - After the grace period is used up, late submission results in a zero grade
- Zero tolerance for cheating
- Collaboration OK, copying NOT OK
- No extra work for extra credit
- Check class web pages regularly. Students are responsible for checking their email, the discussion threads and the announcements section on class web page regularly

Grading Policy

- **20% Homework and quizzes**
- **20% final project**
  - **Two phases**
  - **Requires a lot of time**
- **25% Midterm - open notes, open book.**
- **35% Final exam - open notes, open book**

Action Required

- **Subscribe to the class email list**
  - **Instructions on class website**
- **Read the definition of academic integrity at:** **http://www1.umn.edu/oscai/**

VLSI Area Courses at the U

VLSI CAD	VLSI Circuits	Others
EE 5301 VLSI Design Automation I	**EE 5323** VLSI Design I	**EE 5327** VLSI Design Lab
EE 5302 VLSI Design Automation II	**EE 5324** VLSI Design II	**EE 5329** VLSI Digital Signal Processing Systems
	EE 5333 Analog Integrated Circuit Design	

- **Plus a wide variety of 8000 level courses**

Course Overview

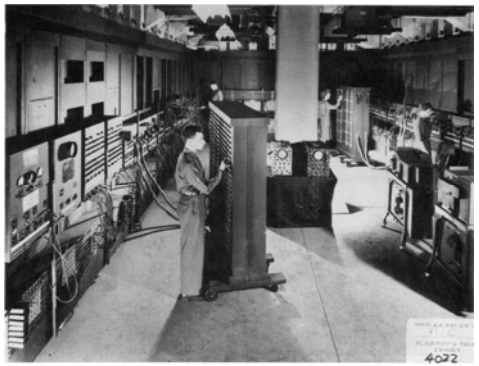
- **This class is intended to be an introduction to the design of very large scale integrated (VLSI) circuits. It is the first part of a two-semester sequence: this part focuses on the transistor-level and logic-level aspects, while the second part, EE 5324, concentrates on designing circuits that implement various functionalities (e.g. memories, datapath units).**
- **The main objective of the two-semester sequence is to provide the student with the capability of designing digital VLSI circuits.**

The First Computer

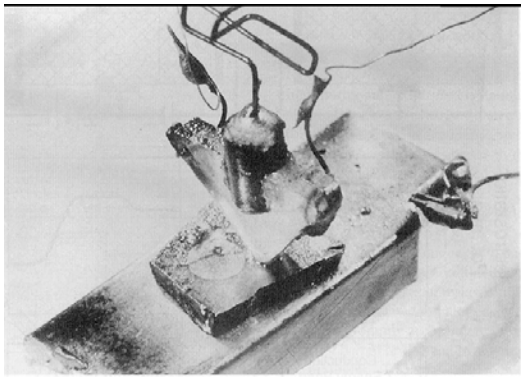
The Babbage Difference Engine (1832)

25,000 parts
cost: £17,470

ENIAC - The First Electronic Computer (1946)

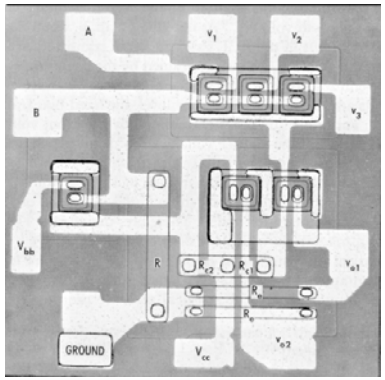


The Transistor Revolution



First transistor
Bell Labs, 1948

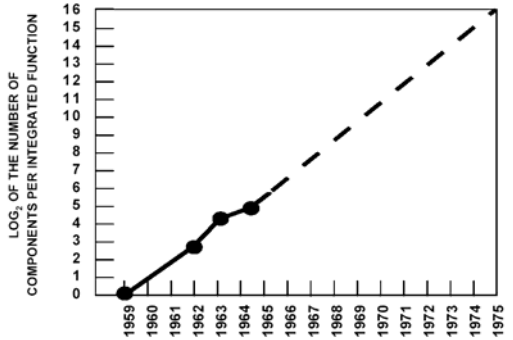
The First Integrated Circuits



Bipolar logic
1960's

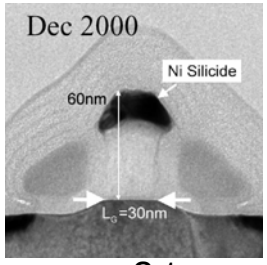
ECL 3-input Gate
Motorola 1966

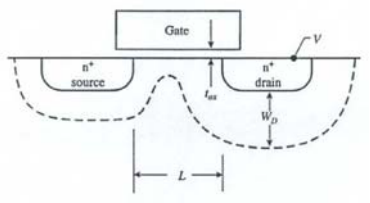
Moore's Law

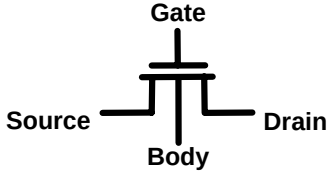


- **Intel founder and chairman Gordon Moore predicted in 1965 that the number of transistors on a chip will double every 18-24 months**

MOS Transistor

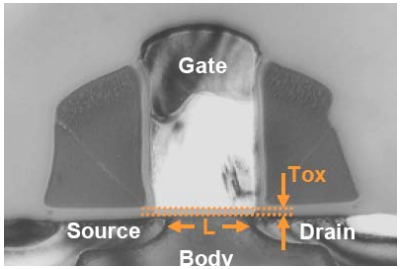


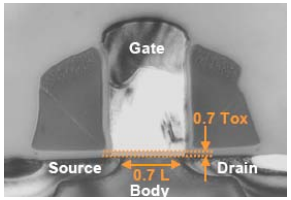




Kuroda, IEDM panel

Transistor Scaling





- Constant Voltage Scaling
- Constant E-field Scaling

Good Old Days: Intel Processors

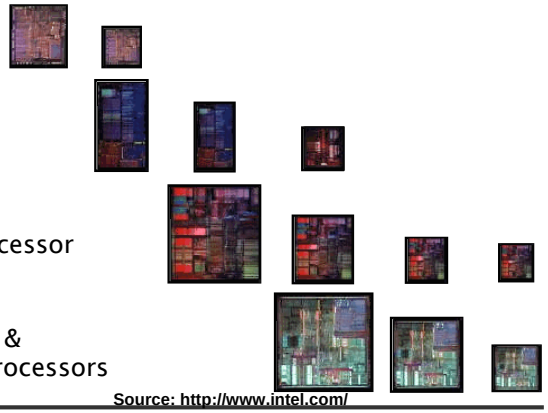
Silicon Process Technology 1.5µ 1.0µ 0.8µ 0.6µ 0.35µ 0.25µ

Intel386™ DX Processor

Intel486™ DX Processor

Pentium® Processor

Pentium® Pro & Pentium® II Processors



Source: http://www.intel.com/

ITRS Roadmap

ITRS roadmap (2002)

Year	2001	2003	2005	2007	2010	2013	2016
DRAM ½ pitch [nm]	130	100	80	65	45	32	22
MPU transistors/chip	97M	153M	243M	386M	773M	1.55G	3.09G
Wiring levels	8	8	10	10	10	11	11
High-perf. phys. gate [nm]	65	45	32	25	18	13	9
High-perf. VDD [V]	1.2	1.0	0.9	0.7	0.6	0.5	0.4
Local clock [GHz]	1.7	3.1	5.2	6.7	10.0	16.9	28.8
High-perf. power [W]	130	150	170	190	218	251	288
Low-power phys. gate [nm]	90	65	45	32	22	16	11
Low-power VDD [V]	1.2	1.1	1.0	0.9	0.8	0.7	0.6
Low-power power [W]	2.4	2.8	3.2	3.5	3.0	3.0	3.0

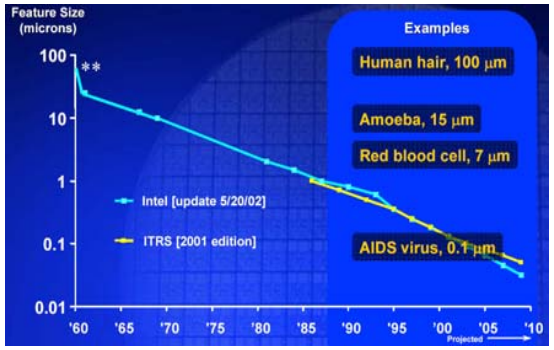
1 B

1 V

2 GHz

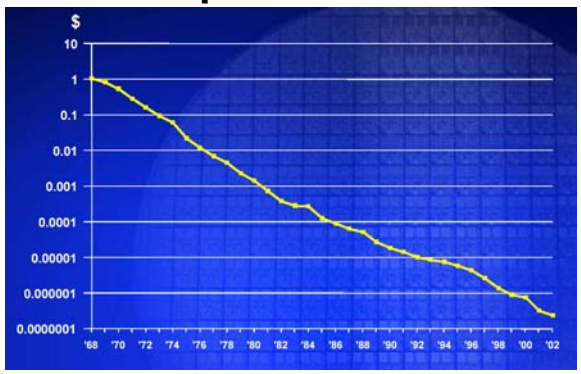
- International Technology Roadmap for Semiconductors 2002 projection (http://public.itrs.net/)

Transistor Scaling



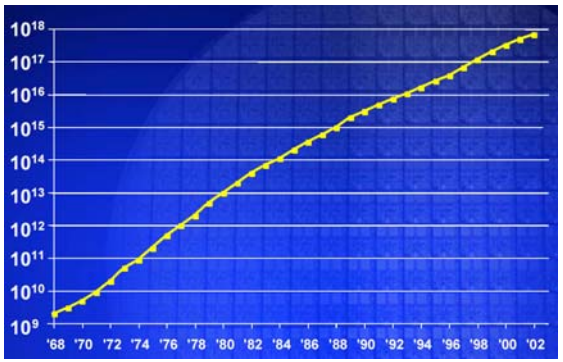
- 45nm is getting ready for production, 32nm is in research phase
- New technology generation introduced every 2-3 years

Cost per Transistor



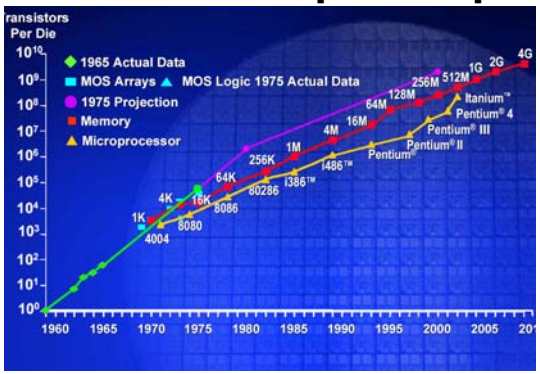
- You can buy 10M transistors for a buck
- They even throw in the interconnect and package for free

Transistors Shipped Per Year



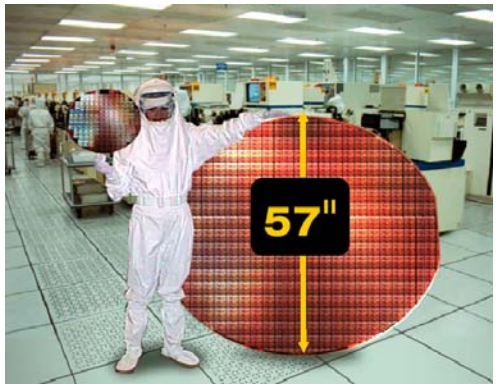
- Today, there are about 100 transistors for every ant
  - Gordon Moore, ISSCC '04

Transistors per Chip

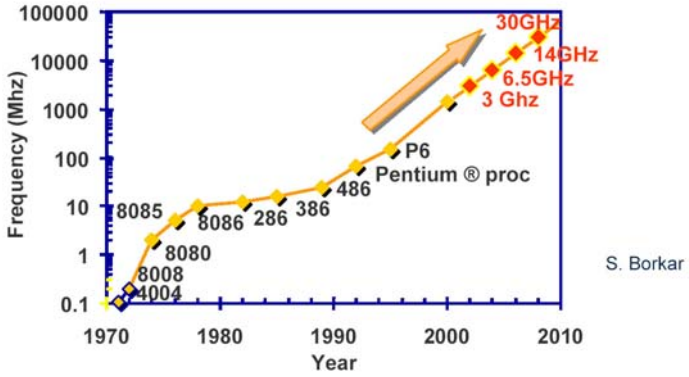


- 1.7B transistors in Montecito (next generation Itanium)
- Most of the devices used for on-die cache memory

Moore's Wrong Prediction

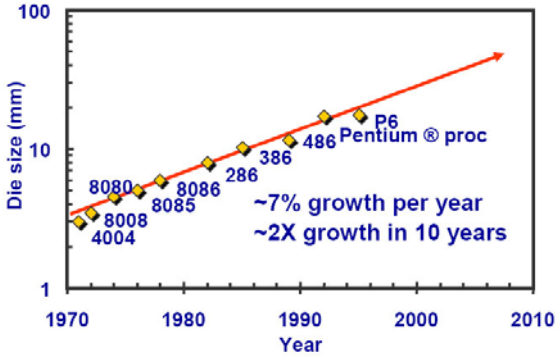


Chip Frequency



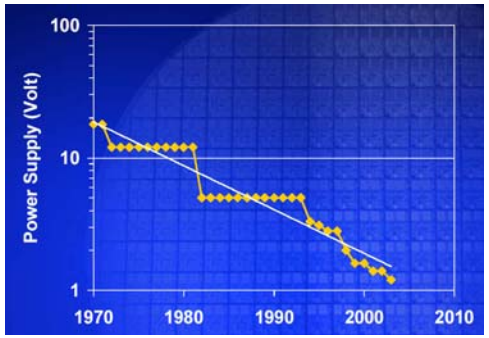
- 30% higher frequency every new generation

Die Size



- ~15% larger die every new generation
- This means more than 2X increase in transistors per chip

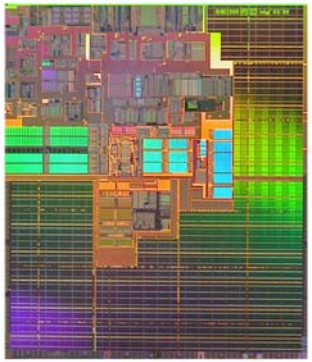
Supply Voltage Scaling



- Supply voltage is decreased for power reduction

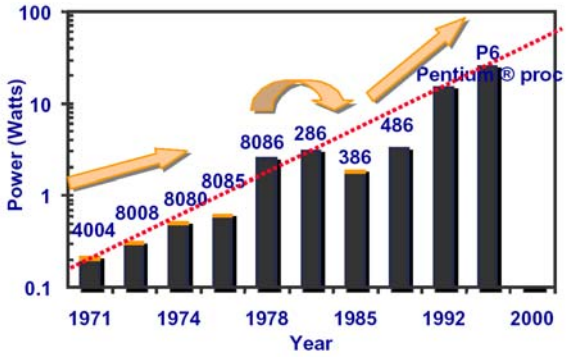
$$P_{active} \propto C V_{dd}^2 f$$

4 Decades of Transistor Scaling:
Itanium 2 Processor



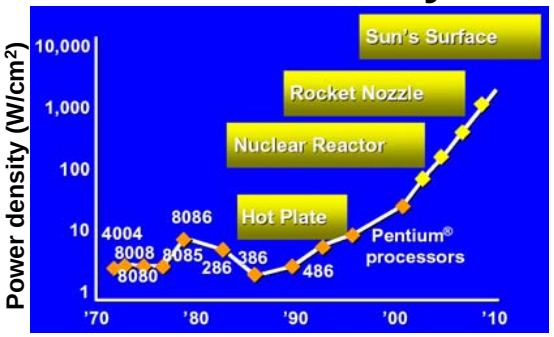
- 130nm process
- 410M transistors
- 374mm² die size
- 6MB on-die L3 cache
- 1.5GHz at 1.3V
- 6.4GB/s 400MT/s 4-way bus interface
- System compatible with existing Itanium 2 platforms
- Extensive RAS, DFT and DFM features

Power



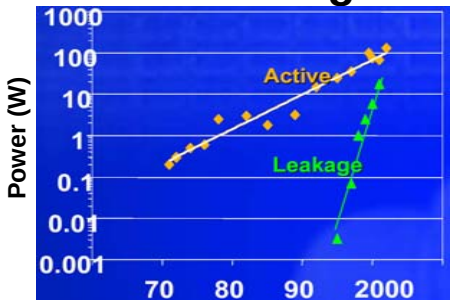
- Lead microprocessors power continues to increase

Power Density



- High-end microprocessors: Packaging, cooling
- Mobile/handheld applications: Short battery life

Active and Leakage Power

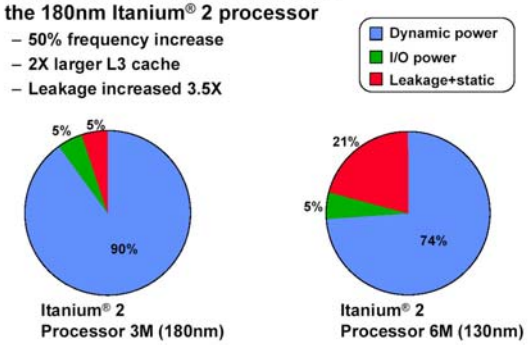


$$delay \propto \frac{C_L}{1 - V_t / V_{dd}} \qquad I_{leak} \propto \exp\left(\frac{-V_t}{mkT/q}\right)$$

- Transistors are becoming dimmers

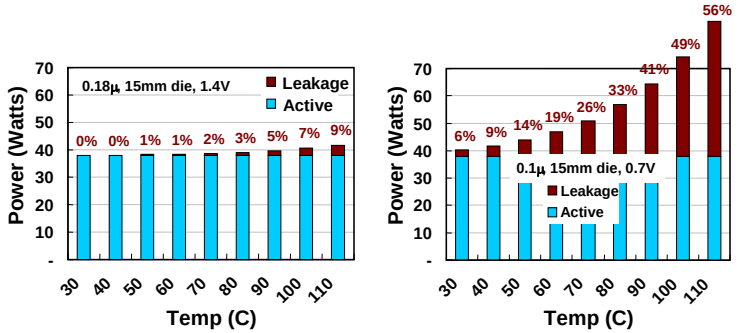
Leakage Power Crawling Up in Itanium 2

- Same thermal design envelope as the 180nm Itanium® 2 processor
  - 50% frequency increase
  - 2X larger L3 cache
  - Leakage increased 3.5X



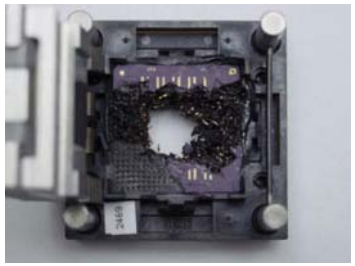
- Transistor leakage is perhaps the biggest problem

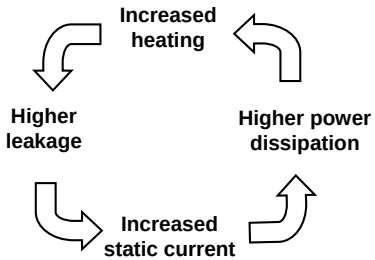
Leakage Power versus Temp.



- Leakage power is problematic in active mode for high performance microprocessors

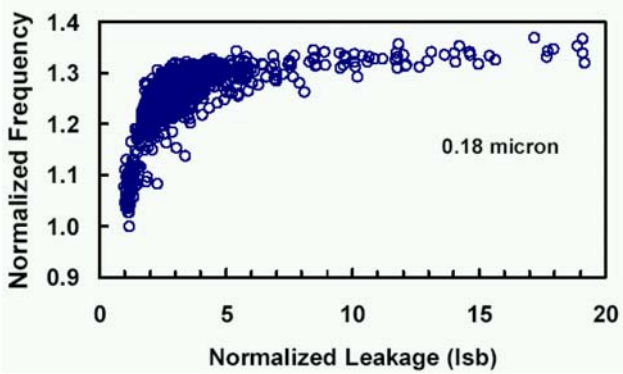
Thermal Runaway





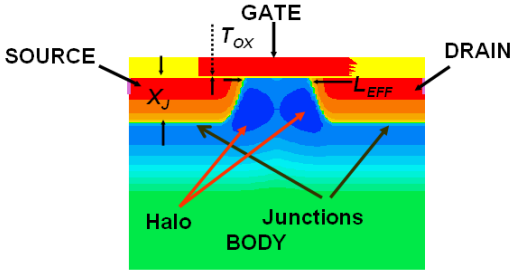
- Destructive positive feedback mechanism
- Leakage increases exponentially with temperature
- May destroy the test socket → thermal sensors required

Process Variation in Microprocessors



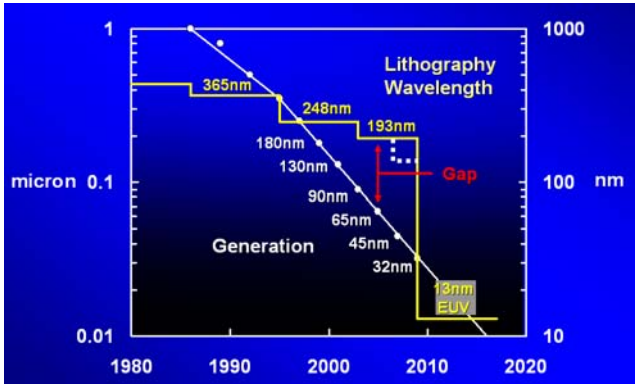
- Fast chips burn too much power
- Slow chips cannot meet the frequency requirement

Sources of Process Variation

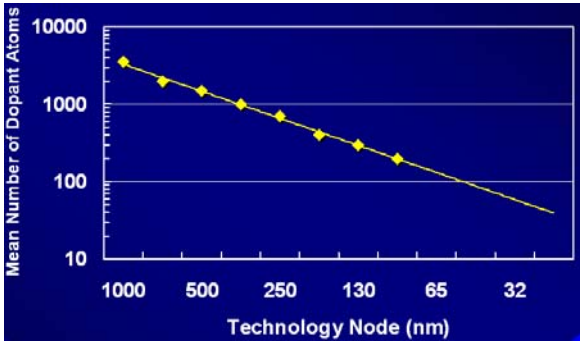


- Intrinsic parameter variation (static)
  - Channel length, random dopant fluctuation
- Environmental variation (dynamic)
  - Temperature, supply variations

Sub-wavelength Lithography

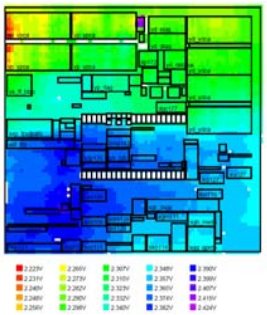


Random Dopant Fluctuation

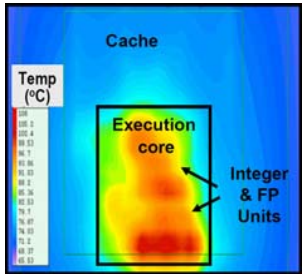


- V_t variation caused by non-uniform channel dopant distribution

Voltage and Temperature Variations

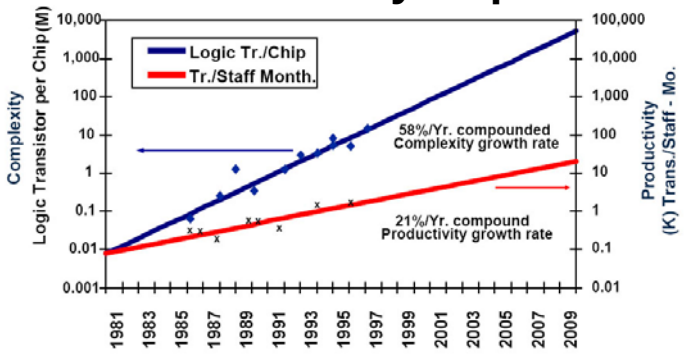


- IR, Ldi/dt noise



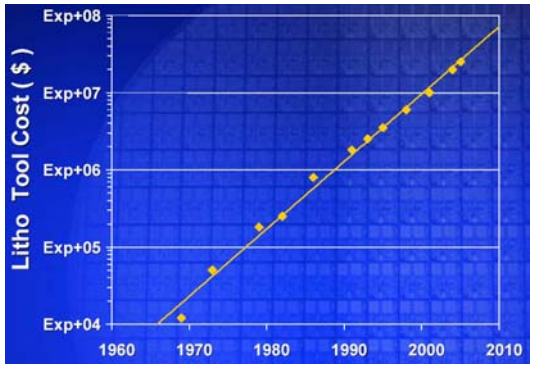
- Hotspot
- Thermal runaway

Productivity Gap



- Design complexity surpasses manpower
- Effective CAD tools, memory dominated chips

Lithography Tool Cost



- What will end Moore's law, economics or physics?

Summary

- Digital IC Business is Unique
  - Things Get Better Every Few Years
  - Companies Have to Stay on Moore's Law Curve to Survive
- Benefits of Transistor Scaling
  - Higher Frequencies of Operation
  - Massive Functional Units, Increasing On-Die Memory
  - Cost/MIPS Going Down
- Downside of Transistor Scaling
  - Power (Dynamic and Static)
  - Process Variation
  - Design/Manufacturing Cost
  - ....