Low Voltage Low Power Dynamic Differential Difference Operational Amplifier

EE 8185 Design Project Proposal

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Objective

Combining conventional analog operational amplifier design methodology with new low voltage, low power technology to implement a low voltage low power (LVLP) differential difference operational amplifier (DDOA) with following parameters:

Parameter Name	Value	Parameter Name	Value
Technology	$1.2\mu m$	Power Supply	$\pm 1.5V$
Open Loop Gain	> 4000	Band Width	100 KHz
CMR	$\pm 1V$	Slew Rate	$\pm 1\frac{V}{\mu s}$
Output Range	$\pm 1.2V$		

The idea is using advanced analog design methodology for LVLP to push the basic analog circuit design toward LVLP applications. It is necessary to point out that this report is just an outline of what the final project will accomplish. Those parameters mentioned above are subjected to be changed during the design process to achieve higher performance or more realistic.

Introduction

Differential difference operational amplifier (DDOA, conventional symbol is shown in Figure 1.) is a

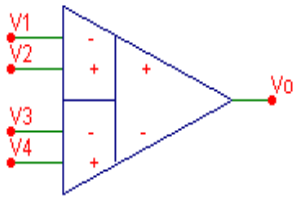

Figure 1

useful block for analog signal processing. Before discussing the low voltage low power (LVLP) DDOA, a brief refresher of the basic DDOA operational equation is given. As discussed in [1] - [3], the DDOA is an extension of the concept of the op-amp, the main difference being that, instead of two single-ended inputs as in the case of op-amps, it has two differential input ports (V2 - V1) and (V4 - V3). The output voltage of the DDOA can be written as :

$$V_{out} = A_0[(V_2 - V_1) - (V_4 - V_3)] \qquad (1)$$

where A0 is the open-loop gain of the DDOA. When a negative feedback is introduced to V1 and/or V4, the basic equation that characterizes the operation of the DDOA is obtained as:

$$V_2 - V_1 = V_4 - V_3 \qquad with \qquad A_0 \to \infty$$

A similar functional block NMOS realization was discussed [1].

The trends of modern VLSI design is reducing the power dissipation by scaling down the power supply voltage Vdd because a large portion of circuits inside a VLSI chip are digital circuit, dynamic power dissipation component in digital circuits is proportional to the square of the supply voltage, scaling down the Vdd is obviously the most effective way to reduce overall power dissipation, even though it is quite chal-

lenge for analog circuit realization. The realization [1] works for normal power supply (5v) and consumes substantially power thus not suitable for LVLP applications.

Dynamic MOS amplifier is an effective method to achieve LVLP analog design. Copeland and Rabaey first suggested a dynamic MOS amplifier in an inverter form [4]. Later a family of dynamic amplifiers were proposed and their performance was measure by Hosticka [5,6]. The detail characteristic of dynamic amplifiers like settling, slewing and power dissipation is discussed in [7]. The bias current scheme suggested by Hosticka [5] is repeated and shown in Figure 2.

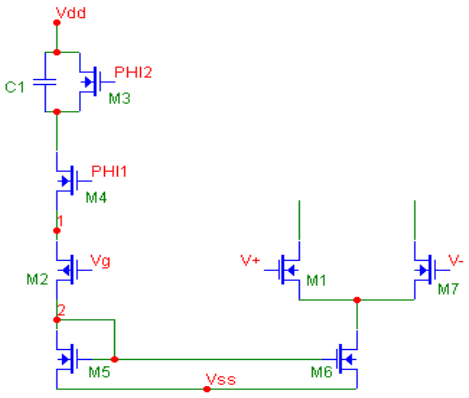

Figure 2.

The circuit operates in the following manner. During PHI2 C1 is discharged and there is no current flowing through transistor M4 and M5. During PHI1 the voltage at node 1 starts at Vdd and rapidly decreases while C1 charges up. Transistor M1 and M7 are the differential input pair of the amplifier. Transistor M2 is not necessary for the basic operation of the bias circuit, however, it serves two important purposes. First, it provides a voltage drop between nodes 1 and 2 during PHI1. If M2 is not include then the initial gate voltage of M5 and M6 will be equal to the supply voltage (Vdd). Therefore, the minimum voltage across M6 before it goes out of the saturation region is equal to Vdd - Vtn. This severely limits the minimum common-mode voltage of the amplifier. Second, the gate voltage and size of M2 can be adjusted to tailor the bias current. If we assume that transistor M2 is in the saturation region, one can easily derive the following equation for the bias current:

$$I(t) = \frac{I_p}{2\left(1 + \frac{t}{t_0}\right)}$$

$$I = \frac{1}{2K_p} \times \frac{W_2}{L_2} \times \Delta V^2$$

where

$$t_0 = (C_1 \cdot \Delta V)/I_p$$

$$\Delta V = V_{DD} - V_g + V_{Tn}$$

The current behavior can be totally described by two parameters: the peak current Ip and the time constant t0. As long as transistor M2 is in the saturation region, the size of M5 has virtually no effect on the current behavior. One can ensure that M2 remains in saturation by setting Vg > V2max + Vtp. V2max can be made to be approximately equal to Vtn by maintaining a large W/L ration for M5. Providing a large ratio for M5 has the additional advantage that the common-mode input range for the opamp is maximized.

Proposed Architecture

The tentative proposed architecture of LVLP DDOA is depicted in figure 3. Two dynamic pre-amplified

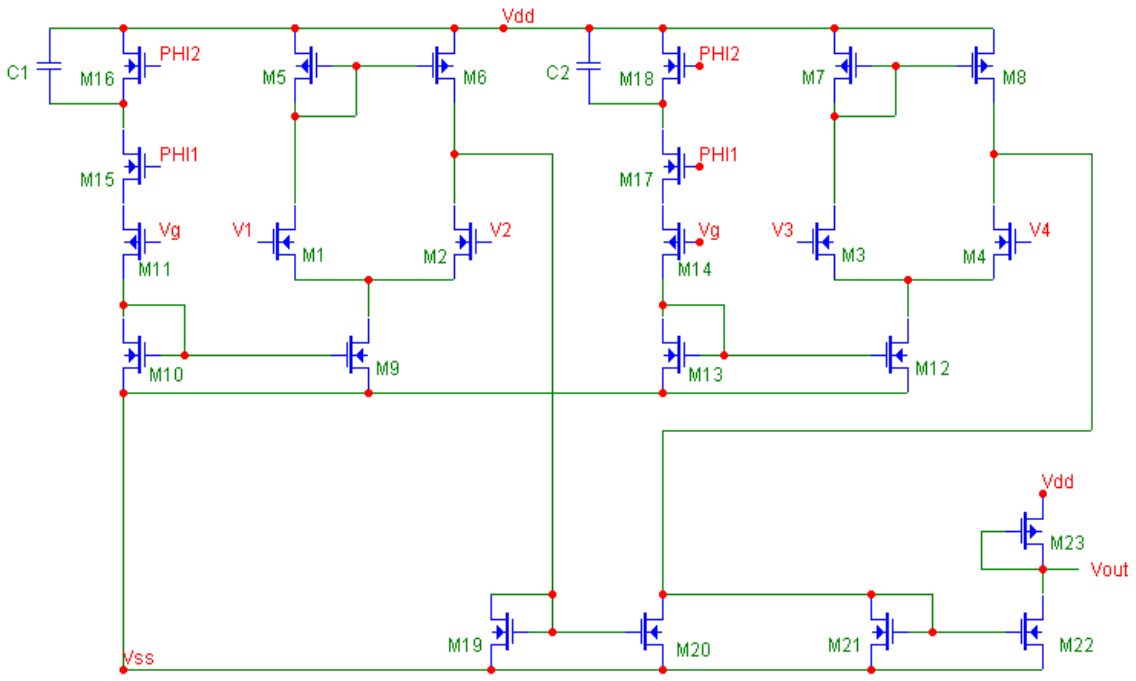

Figure 3

stages are used to generate two differential current signal base on four differential input voltage signals. One current amplifier is used as second amplification stage. It is necessary to point out that the architecture is just a preliminary desing, there must be some compensational or additional circuits are omited tenta-

tively. The structure of this design may also change dynamically along with the design progresses to achieve real LVLP realization.

Next Step

The next step of this project is to determine the critical parameters of this LVLP DDOA such as DC bias, compensation circuit. Then physical dimensional parameters will be determined. Simulation result and comparison to similar circuit will be presented.

References

[1] E. Sackinger and W. Guggenbuhl, "A versatile building block: The CMOS differential difference amplifier," IEEE J. Solid-State Circuits, vol. SC-22, pp. 287-294, Apr. 1987

[2] S.C. Huang, M.Ismail, and S.R. Zarabadi, "A wide range differential difference amplifier. A basic block for analog signal processing in MOS technology," IEEE Trans. Circuits System II, vol. 40, pp. 289-300, May 1993.

[3] J. F. Duque-Carrillo, G. Torelli, R. Pere-Aloe, J. M. Valverde, and F. Maloberti, "Fully differential basic building block based on fully differential difference amplifiers with unity-gain difference feedback," IEEE Trans, Circuits System I, vol. 42, pp. 190-192, Mar, 1995.

[3] Soliman A. Mahmoud and Ahmed M. Soliman, "The Differential Difference Operational Floating Amplifier: A New Block for Analog Signal Processing in MOS Technology," IEEE Trans, Circuits and Systems II, vol. 45. pp. 148-157, Jan, 1998

[4] M. A. Copeland and J. M. Rabaey, "Dynamic amplifier for MOS technology," Electron Lett., pp. 301-302, May 1979.

[5] B. J. Hosticka, "Dynamic CMOS amplifiers," IEEE JSC, pp. 887-894, Oct. 1980

[6] B. J. Hosticka, "Performance of integrated dynamic MOS amplifiers," Electron Lett., pp. 298-300, Apr. 1981.

[7] Feng Wang and Ramesh Harjani, "Dyanmic Amplifiers: Settling, Slewing and Power Issues,".