

--- University of Minnesota ---
 Institute of Technology
 Department of Electrical Engineering

Midterm#2

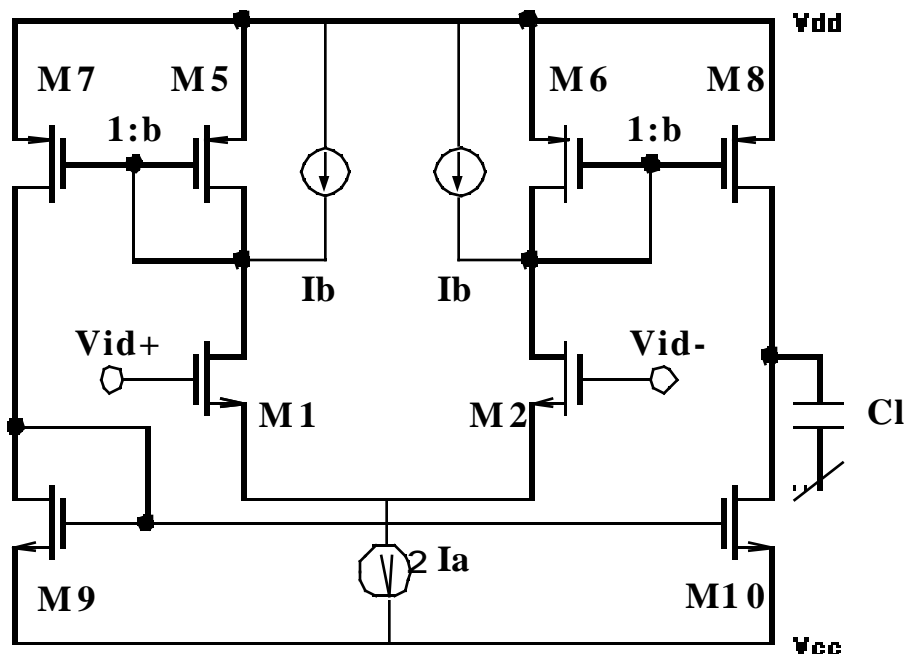
Open book, open notes, take home
 To be handed out November 20, 1998

To be returned November 23, 1998 (before start of class)

EE5505: Analog Integrated Circuit Design

Fall 1998

- 1) This is a design problem. However before completing the design we are required to complete the analysis. For each question show your work and also put down the device numbers associated with each circuit parameter. For example when referring to the transconductance of M5 refer to it as gm5. The bottom current mirror (M9 and M10) have a gain of 1. Let $L_0 = 1.2\mu\text{M}$ (minimum process length). Let $\lambda_{D0} = 0.03$. Let $W_0 = 1.8\mu\text{M}$ (minimum process width). Let $\text{tox}=300\text{\AA}$. Let $K_n=46\text{e-}6$, Let $K_p=19\text{e-}6$. Let $K_{Fp}=5\text{e-}25$ and $K_{Fn}=1.2\text{e-}23$. (K_{Fp} and K_{Fn} are the ones used in HSPICE)



- a) For the circuit on the previous page derive an expression for the small-signal low frequency gain in terms of transconductances and output conductances. (5points)
- b) Next develop the same expression in terms of device geometries and bias currents (2points)
- c) Find an expression for the unity gain frequency of this circuit. (5points)
- d) Find an expression for the slew-rate of the amplifier (5points)
- e) Find an expression for the input common-mode range in terms of ΔV_{GS} and threshold voltages. (5points)
- f) Find an expression for the output common-mode range in terms of ΔV_{GS} and threshold voltages. (5points)
- g) Find an expression for the input referred noise of this circuit. Let the noise for the bias current network be equal to I_{a^2} and I_{b^2} respectively. (5 points)
- h) Find an expression for the non-dominant pole in this circuit in terms of device capacitances, transconductances and output conductances (5 points)
- i) For $I_b = 0.5 \cdot I_a$ design a circuit that has the following characteristics. Design a circuit that gives you the minimum power and area. Show all steps for each characteristics. Give all device geometries. Set $b = 3$. (50 points)

$$C_l = 10 \text{ pF}$$

$$\text{Slew-Rate} = 5 \text{ V}/\mu\text{s}$$

$$V_{DD} = 5.0$$

$$V_{SS} = 0.0$$

$$UGF = 1.2 \text{ MHz}$$

$$\text{Gain (low frequency)} \geq 60 \text{ dB}$$

$$V_{omax} = 4.5 \text{ V}, V_{omin} = 0.5 \text{ V}$$

$$V_{inmin} = 1.0, (\text{let } \Delta V_{GS} \text{ of } I_a = 0.3 \text{ V})$$

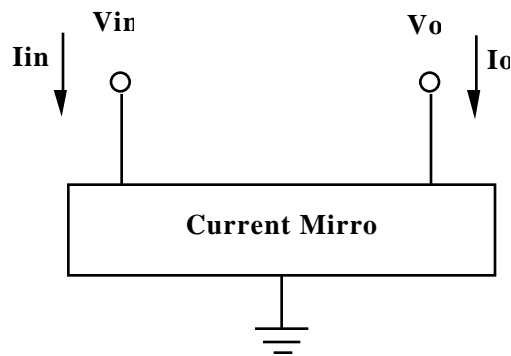
$$V_{inmax} = 4.0, (\text{let } \Delta V_{GS} \text{ of } I_b = 0.3 \text{ V})$$

$$\text{Input referred noise from } 0.1 \text{ Hz to } 1 \text{ kHz} \leq 15 \mu\text{V}.$$

- j) EXTRA CREDIT (confirm your results with SPICE (Use the model parameters and the end of the paper. These are the same as those on my web-site.)) (10 points)

- 2) For this question use the parameters given below. Design a CMOS current mirror that meets the following set of specifications. Assume that the input and output nodes, shown in the figure below, are connected to ideal current sources with no capacitive or resistive components. Also assume that the common source terminal is connected to the ground node. Neglect thermal noise and drain-to-bulk capacitance. Select the appropriate current mirror topology and calculate the required device sizes. **[15 points]**

small-signal output resistance r_o	$\geq 10 \text{ Meg } \Omega$
minimum output voltage range $V_{o\min}$	$= 0.5 \text{ V}$
output flicker noise current @ 100Hz	$\leq 75.6 \text{ pA}/\sqrt{\text{Hz}}$
output pole frequency (3dB freq)	$\geq 50 \text{ MHz}$
quiescent current I_{in}	$= 20 \mu\text{A}$



$$\lambda = \frac{\lambda_{\min} * L_{\min}}{L}$$

where L_{\min} is the process minimum length.

$$\lambda_{\min} = 0.2$$

$$k'_{n\text{mos}} = 40\text{E-}6$$

$$k'_{p\text{mos}} = 15\text{E-}6$$

$$L_{\min} = 4\mu\text{m}$$

$$W_{\min} = 4\mu\text{m}$$

$$C_{gd} = C_{GD0} * W$$

$$C_{GD0} = 3\text{E-}10$$

$$\epsilon_{\text{ox}} = 3.5\text{E-}11 \text{ Farads/Meter}$$

$$T_{\text{ox}} = 400\text{\AA}$$

$$C_{gs} = \frac{2}{3} (L * W * C_{\text{ox}})$$

$$e_{\text{eq}}^2(\text{flicker}) = \frac{\text{KF}}{2 * f * C_{\text{ox}} * W * L * k'}$$

gate referred flicker noise voltage

$$\text{KF} = 2.5\text{E-}27$$

SPICE MODEL to be used for simulation purposes

*N86O SPICE LEVEL3 PARAMETERS

* Copied from MOSIS website 9/22/98 (models extracted Aug 98)

.MODEL CMOSN NMOS LEVEL=3 PHI=0.700000 TOX=3.1600E-08 XJ=0.200000U TPG=1
+ VTO=0.6488 DELTA=1.3120E+00 LD=1.1000E-09 KP=7.4931E-05
+ UO=685.7 THETA=1.0510E-01 RSH=1.4430E+01 GAMMA=0.6375
+ NSUB=1.4620E+16 NFS=7.1250E+11 VMAX=1.9690E+05 ETA=8.7220E-02
+ KAPPA=1.7070E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.3679E-10 CJ=2.8467E-04 MJ=5.1265E-01 CJSW=1.2852E-10
+ MJSW=1.0000E-01 PB=9.6031E-01

* $W_{eff} = W_{drawn} - \Delta W$

* The suggested ΔW is 8.8200E-07

.MODEL CMOSP PMOS LEVEL=3 PHI=0.700000 TOX=3.1600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7917 DELTA=2.6770E+00 LD=9.1170E-10 KP=1.9473E-05
+ UO=178.2 THETA=1.0930E-01 RSH=1.2190E+00 GAMMA=0.3303
+ NSUB=3.9240E+15 NFS=6.4990E+11 VMAX=1.8190E+05 ETA=1.3250E-01
+ KAPPA=9.0000E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.2839E-10 CJ=2.8734E-04 MJ=4.3663E-01 CJSW=1.6570E-10
+ MJSW=1.0000E-01 PB=7.6293E-01

* $W_{eff} = W_{drawn} - \Delta W$

* The suggested ΔW is 8.4240E-07