Stress-based Electromigration Modeling in IC Design: Moving from Theory to Practice

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***Abstract*—Recent research has shown that current density-based models for electromigration (EM) lack precision and should be replaced by physics-based hydrostatic stress simulation. While this new approach is widely accepted in the research community, it has not yet found its way into mainstream IC design flows. This paper aims at bringing state-of-the-art stress-based EM modeling into practical IC design. This is achieved by first examining the reasons that prevent the use of stress modeling in today's verification flows, and then proposing solutions that address these obstacles, such as extracting the necessary technology information from standard IC lifetime testing. The proposed stress modeling approach is used to calculate the EM lifetime for example structures based on equivalent RC circuits, using common IC design tools. Finally, the presented approach is further verified by implementing reservoirs for extending interconnect lifetime.**

***Index Terms*—Electromigration, Stress, IC design, Lifetime**

I. Introduction

Electromigration (EM) is a key concern for integrated circuit (IC) reliability. In interconnects that suffer from EM-induced degradation, voids can occur and cause circuit malfunction or complete failure. To prevent this, process design kits (PDKs) contain temperature-dependent current density limits for short length and long interconnects; these limits are obtained by lifetime measurements on large arrays of test structures [1].

EM modeling has been extensively researched in recent years. It is widely agreed that the conventional current density verification lacks precision and leads to large safety margins and severe over-design, resulting in (unnecessarily) increased chip area (as current density is reduced by widening wires).

Addressing these drawbacks and facing the growing EM issues in small technology nodes, newer models are based on stress evolution (so-called *stress-based* or *physics-based EM modeling* widely associated with Korhonen [2]) with the following advantages:

- capturing the dependency of EM lifetime on wire length,
- handling multi-segment and/or branched interconnects with different current density in each segment, and
- implementing targeted measures enhancing EM lifetime.

Despite the enormous advantages that stress-based EM models offer to IC design and reliability, they have not found their way into PDK models, design tools, and thus, IC design flows. While in the EM modeling community, stress-based EM lifetime verification is considered the state of the art, IC designers and reliability engineers typically use the empirical models provided in PDKs and are only partly aware of these new modeling methodologies and their possibilities.

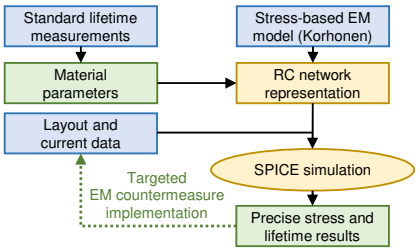

Fig. 1. Overview of our proposed flow on how to apply stress-based EM modeling in IC design. Blue boxes correspond to existing data and models, yellow boxes to recent EM modeling methods, and green boxes highlight the contributions of this paper.

To our knowledge, there are three main obstacles preventing the use of stress-based EM verification in IC design: (1) Stress-based models require technology information (i. e., material parameters) that are not provided in standard PDKs. (2) There are no established IC design tools that support stress-based modeling. (3) Scientific publications on stress-based modeling methods come with little to no hands-on instruction on how to implement them in an IC design flow.

This paper aims to close the gap between state-of-the-art stress-based EM modeling and IC design by directly addressing these obstacles. In Section II, we introduce the basics of stress-based EM modeling. In Section III, we first propose a method for estimating material parameters from standard EM lifetime measurements (Section III-A), and then present an approach for lifetime calculation using RC networks and SPICE (Section III-B). Since IC designers are familiar with RC models and extensively use SPICE, this method can be intuitively understandable to IC designers and, hopefully, lowers the barrier of using stress-based methods. Finally, we show an example of how and where we can implement reservoirs to counteract EM using RC network models (Section III-C). Figure 1 illustrates how these steps are integrated in an EM verification flow.

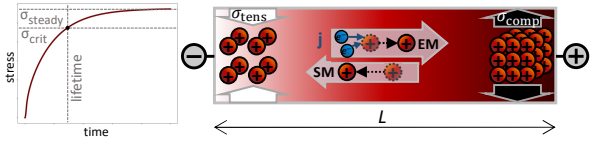

Fig. 2. The basic principle of stress evolution in a single-segment line [1]: driven by EM, atoms are pushed from the cathode toward the anode of the wire. The resulting stress gradient causes stress migration as a counteracting force. The tensile stress at the cathode can lead to voids, and the compressive stress at the anode can cause extrusions. In this paper, we focus on voids as the most common EM failure mechanism. The graph on the left shows stress evolution at the cathode end of the wire. If $\sigma_{\text{crit}} > \sigma_{\text{steady}}$, the wire is considered immortal. If, as in this example, $\sigma_{\text{crit}} < \sigma_{\text{steady}}$, the wire will fail when the critical stress is reached.

II. EM Modeling

A. From Current Density to Stress

In today's IC design flows, EM modeling relies on two steps: (1) A maximum current density limit for general interconnects is determined using the empirical Black's equation [3]. (2) For short wires, a higher current density limit based on the Blech equation [4] is permitted.

Black's model is suitable for estimating the allowed current density to ensure a targeted lifetime, but it completely ignores interconnect geometry (e. g. wire length dependency). For very long wires, length indeed has negligible impact on lifetime, but Black's model is known to be highly pessimistic for wires of moderate length (see Sec. III).

The Blech model checks for "immortal" wires. In PDKs, it is applied to short wires in which the maximum (steady-state) hydrostatic stress, σ_{steady}, does not exceed the critical stress, σ_{crit}, for voiding.

A common feature of both models is that they are designed for single-segment interconnects stressed with a uniform current density. However, realistic layouts have more complex interconnect geometries (e.g., multiple segments) and different current densities in each wire segment. Thus, applying the models mentioned above to realistic interconnect structures either requires unnecessarily high safety margins or severe underestimation of the actual EM risk [5].

State-of-the-art EM models are based on the Korhonen equation and its extensions to multi-segment interconnects. This equation, with boundary conditions (BCs), for a finite line describes the evolution of stress, σ, over time, t, as follows:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} - \beta j\right)\right], \text{ BCs: } \left.\frac{\partial \sigma}{\partial x}\right|_{x=0,L} = \beta j \quad (1)$$

where j is the current density, $\kappa = DB\Omega/k_{\text{B}}T$, $\beta = e\rho Z/\Omega$, diffusivity $D = D_0 \cdot \exp\left(-E_{\text{a}}/\left(k_{\text{B}}T\right)\right)$, B is the Bulk modulus, Ω the atomic volume, k_{B} Boltzmann's constant, T the Temperature, e the elementary charge, ρ the specific resistivity, Z the electric charge number, D_0 the diffusion constant, and E_{a} the activation energy.

For a finite line of length L, the solution to this equation at a distance x from the cathode, at time t, is given by [2]:

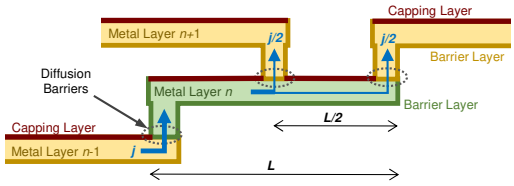

Fig. 3. Illustration of our example in Section III-B in the context of a dual damascene process. We calculate the stress in the green wire, which is part of a more complex net. The diffusion barriers formed by the capping layers allow us to separate the net into stress-wise independent interconnects.

$$\sigma(x,t) = \beta j L\left(0.5 - \frac{x}{L} - 4\sum_{m=0}^{\infty}\frac{\cos((2m\pi+\pi)\frac{x}{L})}{(2m\pi+\pi)^2 \exp\left((2m\pi+\pi)^2\kappa\frac{t}{L^2}\right)}\right) \quad (2)$$

The above equation enables us to calculate hydrostatic stress evolution in a wire over time. Wire robustness verification with these models detects voiding by comparing σ against the critical stress, σ_{crit}. First, interconnects can be checked for their immortality, invoking the Blech criterion [4] for single-segment interconnects with constant current density, or extensions for multi-segment interconnects with different current densities in each segment [6]. Wires are considered immortal when the steady-state stress at every location of the wire remains lower than the critical stress. However, in many cases, the steady state is not reached within the lifetime of the chip that contains the wire. Therefore, even for "mortal" wires, the EM robustness can be verified by checking that the critical stress is not exceeded within the specified lifetime (Fig. 2) [7].

B. Equivalent RC Networks for Multi-segment Interconnects

Several methods have been proposed in the literature for solving Korhonen's equations for general multi-segment interconnects. In this paper, we will focus on equivalent RC networks because they are intuitively understandable for IC designers and are easy to solve using SPICE simulations. Detailed information on this method can be found in [8], [9].

In dual-damascene processes, metal layers are separated by diffusion barriers and, thus, we can assume mass conservation for the individual interconnect structures and zero atomic flux at their connection points (i. e., vias) toward other layers. Therefore, in the first step, we split nets into interconnect structures lying within one metal layer. Second, the interconnect structure is divided into smaller elements (discretization), each with length Δx, width w and height h. Each of these elements is represented by a RC-π-structure, modeled as follows:

$$R = \Delta x/(w \cdot h \cdot \kappa), \; C = \Delta x \cdot w \cdot h. \quad (3)$$

In the third step, current loads i_{EM} are applied as current sources at every point where a current i_{IC} flows into or out of the interconnect with

$$i_{\text{EM}} = \kappa \cdot \beta \cdot i_{\text{IC}}. \quad (4)$$

In practice, this corresponds to a current source at every via.

This RC structure can be solved using standard electrical techniques. By construction, the voltages in this RC structure

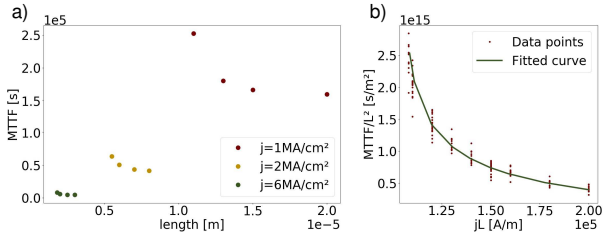

Fig. 4. a) Lifetime FEM results, b) Data points with added noise and curve fitting result.

map on to the stress at the corresponding nodes in the wire. With an initial condition of zero voltage at every node (for zero initial stress) the circuit can then be simulated in SPICE, and the transient voltage results correspond to the temporal profile of EM-induced stress evolution.

III. Stress-based EM Modeling in IC Design

All scripts used to obtain the results presented in this section are available online [10].

A. Finding Material Parameters

In order to apply stress-based EM modeling it is crucial to know the material parameters of the technology, i. e., κ, β, and σ_{crit}. These are not provided in PDKs and, to the best of our knowledge, not characterized by the fabs today.

In standard EM tests, single-segment wires with length L are stressed with a current density j to determine their lifetime. Based on these measurements, Black's equation, and the Blech criterion, the allowable current densities are determined, depending on the required lifetime after appropriately scaling accelerated aging conditions to normal conditions [11].

Conducting these measurements on mortal wires of different lengths will result in a dataset that captures the dependency of the lifetime on the current density and wire length, as illustrated in Fig. 4a. For the applied current density j, these measurements must cover the length range from just above the longest immortal wire length (where $jL = (jL)_{\text{max}}$) to long wires (where length only minimally impacts the lifetime).

In a single-segment line, the stress profile is symmetric and the maximum stress will occur at the two ends of the wire. Thus, at the moment of failure, we can expect the stress at the end of the wire to equal the critical stress, $\sigma(x = 0, t_{\text{life}}) = \sigma_{\text{crit}}$. Substituting this into eq. (2), and solving for jL yields

$$jL = \frac{\sigma_{\text{crit}}}{\beta}\left(0.5 - 4\sum_{m=0}^{\infty}\frac{\exp\left(-(2m\pi+\pi)^2\kappa\frac{t_{\text{life}}}{L^2}\right)}{(2m\pi+\pi)^2}\right)^{-1} \quad (5)$$

From eq. (1), since β and σ are linearly related, we can normalize σ to β. Formally, setting $\sigma' = \sigma/\beta$, eq. (1) becomes $\frac{\partial\sigma'}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial\sigma'}{\partial x} - j\right)\right]$; BCs: $\left.\frac{\partial\sigma'}{\partial x}\right|_{x=0,L} = j$. The nucleation criterion $\sigma = \sigma_{\text{crit}}$ becomes $\sigma' = (\sigma_{\text{crit}}/\beta)$. Thus, it suffices to know the ratio between σ_{crit} and β and not their individual values, i.e., we only characterize κ and $(\sigma_{\text{crit}}/\beta)$.

To obtain these parameters, we can use eq. (5) for curve fitting. Terminating the infinite sum at $m = 1$ will ensure

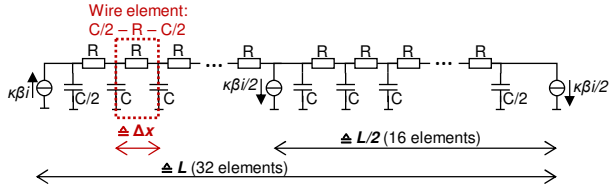

Fig. 5. Equivalent RC circuit for our example in Section III-B. Not all π-elements are shown, we divided the two wire segments in 16 elements, each.

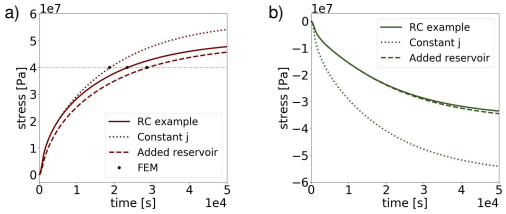

Fig. 6. SPICE results at a) $x = 0$ (cathode) and b) $x = L$ (anode) for our example of a two-segment wire, the case with constant current density j for the whole wire for comparison, and our example with a reservoir added to the cathode end at $x = 0$. The stress axis corresponds to the voltage results from the simulation. The results fit well with FEM, the points marked with dots are the FEM lifetime results.

reasonable precision. We write each of our data points (Fig. 4)[1] as $[t_{\text{life}}/L^2, jL]$ and understand eq. (5) as $jL = f(t_{\text{life}}/L^2)$ to find κ and $(\sigma_{\text{crit}}/\beta)$ using the python `curve_fit`-function (from SciPy). Figure 4b shows lifetime normalized to L^2 as a function of jL and how the obtained curve indeed fits the data points. We conducted our lifetime simulations with $\kappa = 1.35 \cdot 10^{-16}\,\frac{\text{m}^2}{\text{s}}$ and $\sigma_{\text{crit}}/\beta = 5.20 \cdot 10^4\,\frac{\text{kgPa}}{\text{s}^2\text{A}}$ and obtained $\kappa = 1.38 \cdot 10^{-16}\,\frac{\text{m}^2}{\text{s}}$ (error of 2.2%) and $\sigma_{\text{crit}}/\beta = 5.29 \cdot 10^4\,\frac{\text{kgPa}}{\text{s}^2\text{A}}$ (error of 1.7%) as our interpolation results.

B. Estimating Lifetime using SPICE Simulation

Consider the example in Fig. 3 where the EM lifetime of a two-segment line with current density j in the first segment and $j/2$ in the second segment is to be estimated. In practice, designers typically use one of two approaches to apply the current-density boundaries to this simple configuration, both leading to incorrect results: (1) Taking the total length L (to decide whether to apply short length or standard constraints) and the maximum current density j to compare it with the boundaries given in the PDK; this would be pessimistic, as the second segment is stressed with lower current density. (2) Verifying the two segments independently, taking $L/2$ as wire length and j and $j/2$ as current densities; this approach would underestimate the EM risk as the stress of the two segments will "add up" in reality.

Knowing the material parameters κ and $(\sigma_{\text{crit}}/\beta)$, we can now apply the method in Section II-B to this example in two steps:

(1) We build the equivalent RC circuits shown in Fig. 5. Each node voltage corresponds to the node stress σ; to find σ', we exploit the linearity of the circuit: scaling all excitations by a factor $(1/\beta)$ provides node voltages of $\sigma/\beta = \sigma'$.

[1]For our work, we did not have access to real measurement data. To simulate realistic lifetime results, we performed FEM simulations (Fig. 4a) and added random noise (10 % standard deviation) to generate 10 data points for each of our FEM simulation results [10].

Therefore, we use eq. (3) for the RC values, and apply $i_{EM} = \kappa i_{\text{IC}}$, scaling the current excitation by $(1/\beta)$. Void nucleation is detected by comparing σ' at each node against the characterized $(\sigma_{\text{crit}}/\beta)$ value from Section III-A. Both wire segments are divided into 16 elements [9].
(2) We run the transient SPICE simulation and check the nucleation criterion, $\sigma' = (\sigma_{\text{crit}}/\beta)$. If the nucleation time exceeds the targeted lifetime, the wire can be classified as EM-robust. If V_{crit} is not reached at all, the wire is EM-safe.

Figure 6 shows the results that were obtained with σ_{crit} set to 40 MPa and the extracted parameters, $\kappa = 1.35 \cdot 10^{-16}\,\frac{\text{m}^2}{\text{s}}$, $\beta = 7.69 \cdot 10^2\,\frac{\text{kg}}{\text{s}^2\text{A}}$ (calculated from the extracted $\sigma_{\text{crit}}/\beta = 5.20 \cdot 10^4\,\frac{\text{kgPa}}{\text{s}^2\text{A}}$ and the set value for σ_{crit}), $L = 5\,\mu$m and $j = i_{\text{IC}}/(w \cdot h) = 150\,\mu\text{A}/(50\,\text{nm} \cdot 100\,\text{nm}) = 3\,\text{MA/cm}^2$. The solid lines show stress evolution for the example described above. For comparison, the dotted lines show stress evolution in the same line, but with constant current density j. Assuming a critical stress of 40 MPa, this leads to an underestimation of the lifetime by $\approx 20\,\%$. Depending on the layout, currents, and material parameters, this impact can range from nearly no difference to the point where an immortal wire is falsely classified as mortal. The dots show FEM lifetime results. We provide full FEM results and scripts in [10].

This simple, yet easily extendable example demonstrates the power of stress-based EM modeling.

C. Improving Lifetime

For the case where lifetime requirements are not met for certain interconnects, stress modeling also offers some advantages, particularly for multi-segment lines. It shows exactly where the risk of voiding is highest (i. e., which point of the interconnect reaches the critical stress first, $x = 0$ in the example from Section III-B), and enables us to integrate EM countermeasures [1] at the right place, and check their impact on lifetime. One such measure is the use of reservoirs, i. e. pieces of metal that do not carry current. At a location that would be at risk of voiding, they have the purpose of supplying additional metal atoms.

We can use the method of equivalent RC circuits to model the impact of reservoirs. Like normal current-carrying wires, a reservoir is modeled as an RC network and connected to the corresponding node in the original equivalent circuit. We demonstrate this method by adding one more RC-element $C/2$–R–$C/2$ in our example at the node corresponding to $x = 0$. In the layout, this represents a reservoir of length $L/32 = 0.16\,\mu$m.

The results are shown by the dashed lines in Fig. 6. We can observe that the steady-state stress is reduced at the critical node $x = 0$. Again, assuming $\sigma_{\text{crit}} = 40\,\text{MPa}$, the reservoir increases the lifetime by $\approx 23\,\%$.

This gives us a simple and easy-to-apply method for estimating a reservoir's impact on lifetime and also enables us to assess a reservoir's impact when located at another point of the wire (which might be necessary due to congestion).

IV. Conclusion

Stress-based EM modeling outperforms today's practice of current-density verification in many ways. However, even after years of promising research on these models, they have not found their way into contemporary IC design flows. Facing the increasing design challenges in terms of reliability, we believe that stress-based modeling must finally be applied in IC design.

With this paper, we aim for implementing state-of-the-art stress-based EM modeling in today's IC design. First, we looked at the difficulties preventing the application of stress-based modeling. We found that two of the main challenges are the missing technology information and the lack of tools for stress-based verification. We presented a pragmatic approach of overcoming these challenges by providing a method for estimating the necessary material parameters from standard lifetime testing. We also demonstrated how a recently published method of equivalent RC circuits can be used to run stress-based EM simulation in SPICE. Using a simple example, we presented the advantages of stress-based modeling compared to conventional current-density verification. In order to verify our approach, we showed how reservoirs can be modeled using the RC method and how they can be used to improve lifetime. Our results and scripts are publicly available in [10].

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