Electromigration-Aware Interconnect Design

Sachin S. Sapatnekar
Department of Electrical and Computer Engineering
University of Minnesota
Minneapolis, MN (USA)
sachin@umn.edu

ABSTRACT

Electromigration (EM) is seen as a growing problem in recent and upcoming technology nodes, and affects a wider variety of wires (e.g., power grid, clock/signal nets), circuits (e.g., digital, analog, mixed-signal), and systems (e.g., mobile, server, automotive), touching lower levels of metal than before. Moreover, unlike traditional EM checks that were performed on each wire individually, EM checks must evolve to consider the system-level impact of wire failure. This requires a change in how interconnect design incorporates this effect. This paper overviews the root causes of EM, its impact on high-performance designs, and techniques for analyzing, working around, and alleviating the effects of EM.

CCS CONCEPTS

• **General and reference** → **Reliability**; • **Hardware** → **Metallic interconnect**; **Very large scale integration design**; **Electronic design automation**; **Physical design (EDA)**; **Aging of circuits and systems**; *Analog and mixed-signal circuits.*

KEYWORDS

Electromigration, stress, reliability, power grids, clock networks

ACM Reference Format:
Sachin S. Sapatnekar. 2019. Electromigration-Aware Interconnect Design. In *2019 International Symposium on Physical Design (ISPD '19), April 14–17, 2019, San Francisco, CA, USA.* ACM, New York, NY, USA, 8 pages. https://doi.org/10.1145/3299902.3313156

1 INTRODUCTION

Electromigration (EM) in metal wires is a serious reliability problem in deeply-scaled technologies. EM is induced in wires with high current densities, and can result in an increase in wire resistance over time, eventually leading to an effective open-circuit. EM has long been a significant issue that impacts physical design, and analysis and simulation papers in the EDA community have targeted this phenomenon for many years [11, 37]. It is well known that the impact of EM can be mitigated by using wider wires that reduce the average current density in the wire. The causes and impact of EM are documented in the physical design literature [21, 22], and several physical design techniques are outlined in these papers.

For recent and upcoming technology nodes, several changes have made EM considerations different and more important. First, the emergence of FinFETs and gate all-around FETs, coupled with reduced wire cross sections, has resulted in two factors that exacerbate EM: increased wire current densities and elevated temperatures. Second, in the past, EM checks were primarily directed at the uppermost metal layers, but EM has now become increasingly important in lower metal layers as well. Third, EM is no longer considered to be a problem primarily for long-lifetime parts, e.g., in the automotive market, but is also a serious consideration over shorter lifetimes, e.g., in the mobile market. Fourth, unlike traditional EM checks that are performed on a per-wire basis, system failure analysis must incorporate the inherent redundancy of many EM-sensitive interconnect systems.

2 EM ANALYSIS

When a sufficiently high current flows through an on-chip wire over a long period of time, it can cause a physical migration of atoms in the wire. The current-conducting electrons form an "electron wind," which leads to momentum exchange with the constituent atoms of metal. This effect will result in a net flux of metal atoms in the direction of electron flow (opposite of current direction), creating voids (depletion of material) upstream and hillocks (accumulation of material) downstream at locations of atomic flux divergence. EM can cause uneven redistribution of resistance, dielectric cracking, and undesired open circuits. EM is witnessed most notably in supply (power and ground) wires, where the flow of current is mostly unidirectional, but AC EM has been reported in signal wires [19, 38].

We will first overview the basics of EM and then outline both *empirical* EM models based on characterization, and *physics-based* models that capture the dynamics of EM.

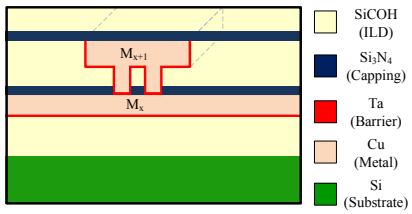

Figure 1: Schematic of dual damascene copper interconnect.

2.1 The roots of EM

The schematic in Fig. 1 illustrates a copper dual-damascene (Cu DD) interconnect structure used in modern integrated-circuits. The

ISPD '19, April 14–17, 2019, San Francisco, CA, USA

ACM ISBN 978-1-4503-6253-5/19/04…$15.00
https://doi.org/10.1145/3299902.3313156

interconnect is made up of copper and is cladded with Ta barrier layer on the sides and bottom. The top surface is bounded by the Si_3N_4 capping layer, while the inter layer dielectric (ILD), made of low-k material, such as SiCOH lies between the copper lines. The entire structure rests on a silicon substrate that is a few hundreds of microns thick.

EM degradation in Cu wires occurs due to the nucleation and growth of voids [12, 29], which results in an increase in the wire resistance and ultimately causes functional failure. Fig. 2 illustrates the two driving forces for EM for a wire of length L – the electron wind force due to the flow of a current density j, and the back-stress force generated due to the stress gradient caused by EM-induced mass redistribution. As the movement of migrated atoms is blocked at either end due to the atom-impermeable barrier layer, the electron wind force causes atomic depletion near the cathode, and the resulting tensile stress generated leads to *void nucleation* when the stress exceeds a critical stress, σ_c. Further electron wind force leads to *void growth*, at a rate dictated by drift velocity.

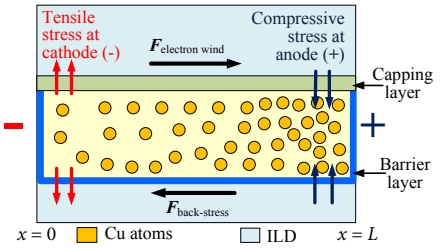

Figure 2: Cross section of a Cu wire indicating the back-stress and the electron wind force.

Korhonen's equation [18] models the temporal evolution of stress, i.e., the interaction between electron wind and back-stress:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\kappa\left(\frac{\partial \sigma}{\partial x} + G\right)\right] \tag{1}$$

Here, the term involving G corresponds to the electron wind force driven by j, $\partial\sigma/\partial x$ relates to the back-stress force, x is the distance from the cathode, and t is the time variable. Other terms are:

$$\kappa = \frac{D_{eff}\, B\, \Omega}{k_B T} \;\; ; \;\; G = \frac{e Z^{\star}_{eff}\, \rho\, j}{\Omega}$$

in which $D_{eff} = D_0 \exp(-E_a/k_B T)$ is the EM effective diffusivity, D_0 is the diffusivity constant, E_a is the activation energy, k_B is Boltzmann's constant, T is the temperature, B is the effective bulk modulus for the metal-ILD system, Ω is the atomic volume for the metal, e is the elementary electron charge, $Z^{\star}_{eff}$ the effective charge number, and ρ is the resistivity.

For the current-carrying line in Fig. 2, the boundary condition is that the net atomic flux at the endpoints enclosed by vias is zero, since the Ta barrier at the vias in a Cu DD process blocks the flow of metal atoms, i.e., $\frac{\partial \sigma}{\partial x} + G = 0$, at $x = 0, x = L$, for all t.

2.2 The Blech criterion

A wire is immortal to EM when the back-stress and electron wind forces are in equilibrium in the steady state, i.e., $\frac{\partial \sigma}{\partial t} = 0$ [6]. Using this condition in (1), if there is no initial stress at $t = 0$,

$$\frac{\partial \sigma}{\partial x} + G = 0 \tag{2}$$

For a constant current flow (i.e., constant G), the slope of the stress profile at steady state is a constant, i.e., $G = \left|\frac{\partial \sigma}{\partial x}\right| = \left|\frac{\Delta \sigma}{L}\right| = \frac{2\sigma}{L}$ [12]. If $\sigma < \sigma_c$, the critical stress that creates a void, the wire will be immortal to EM damage. Therefore,

$$G = \frac{2\sigma}{L} \leq \frac{2\sigma_c}{L} \tag{3}$$

$$\text{i.e., } (j\, L) \leq \frac{2\sigma_c \Omega}{e Z^{\star}_{eff}\, \rho} = (jL)_{\text{crit}} \tag{4}$$

This is the Blech criterion: the product of the current density j and wire length L must not exceed a threshold, $(jL)_{\text{crit}}$.

2.3 Empirical modeling

2.3.1 Black's equation. EM is a statistical process due to variations in the activation energy, E_a, associated with (1). It has been demonstrated that the probability of failure, referred to as the failure fraction FF, follows a lognormal dependency on the time to failure, t_f [5]. Industrial markets demand low failure rates (e.g., 100 defective parts per million (DPPM) over the chip lifetime). Chip reliability engineers translate this chip-level specification to specific fail fraction (FF) targets, in units of failures-in-time (FITs), on individual resistors. The classic Black's equation [5] relates the mean time to failure, t_{50}, to the average current density j across the interconnect cross-section and the wire temperature T as:

$$t_{50} = \frac{A}{j^n} \exp \frac{E_a}{k_B T} \tag{5}$$

Here, A and n are constants and typical values of n are between 1 and 2, since void nucleation and void growth accelerate as $j = 2$ and $j = 1$, respectively [23]. Industry practice involves setting up a current density limit using the above equation for a given target mean time to failure, t_{50}.

It is important to note that the temperature T corresponds to contributions from the ambient temperature as well as RMS-current-induced temperature rise due to Joule heating [14]. Thus the average current determines j, and the RMS current influences T. Before this fact was realized, it was sometimes stated that the exponent n varied between 1 and 3, instead of 1 and 2 as is now accepted.

2.3.2 Using Black's equation. To translate the mean time to failure predicted by Black's equation, the underlying lognormal is used to determine the average current density thresholds to meet a target FF. This is achieved by defining the lognormal transformation parameter (z), which relates t_{50} to the time to failure, t_f, for a specific FF as follows:

$$z = \frac{\ln(t_f) - \ln(t_{50})}{\sigma}, \;\; \text{i.e., } \; t_f = t_{50} e^{\sigma z} \tag{6}$$

$$FF = \int_{-\infty}^{z} \frac{e^{-x^2/2}}{\sqrt{2\pi}} dx \tag{7}$$

where the standard deviation of the distribution, σ, is process-dependent. The transformation variable z helps in directly representing the cumulative failure rate with a normal distribution.

For a given design, the specification provides the acceptable FF and the lifetime of the part, t_{life}. This is translated into a maximum average current density j_{max} as follows:

- The specification is first translated to $t_f \geq t_{life}$. This is a lower bound on t_f.
- Next, the one-to-one mapping between FF and z in Eq. (7) is used to infer z.
- For this z, Eq. (6) translates the lower bound t_{life} on t_f to a lower bound on t_{50}.
- Finally, Black's equation converts the lower bound on t_{50} to an upper bound, j_{max} on the current density j in the wire.

In summary, the conventional empirical method for EM analysis for interconnects involves a two-step process:

- Filtering out EM-immortal wires using the Blech criterion [6]: mortal wires may potentially cause EM failure.
- Checking the current density through these wires against a global limit determined by Black's equation [5].

2.3.3 Pitfalls in characterizing Black's equation. The distribution of t_f is characterized through experiments on interconnect test structures [3], stressed at elevated temperature (typically 300°C [13]) and voltage values, to induce EM failure. The failure times are then mapped back to normal chip operating conditions [23]. The statistical distributions of these test structures capture the variations in EM failure times due to variations in grain structure or activation energy, but fail to capture layout-dependent effects.

Void nucleation occurs when the stress in a wire exceeds σ_c. This stress in a wire could have contributions not only from the electron wind and back stress forces, but also from thermomechanical stress, which is generated due to a mismatch in the coefficient of thermal expansion (CTE) of the metallization and the surrounding dielectric [30]. The CTE differential results in compressive/tensile stresses when the wafer is annealed from high-temperature ($300 - 350$°C) manufacturing conditions to normal operating temperatures. Characterization structures may fail to capture this effect, which a function of the layout and the CTE differentials with the surrounding layers, because (a) they may not be sufficiently diverse to capture all configurations of on-chip interconnects (b) the elevated temperature conditions used during characterization are closer to those at manufacturing [13], due to which thermomechanical stresses are greatly reduced from normal operating temperatures.

2.4 Physics-based modeling

Unlike empirical EM models, physics-based models solve Korhonen's equation, (1). However, the solution takes the form of an infinite series that is expensive to compute. To identify EM-susceptible wires, [27] proposes an efficient filter-based approach.

To present this solution, we consider the solution of Korhonen's equation to compute the stress at the cathode ($x = 0$) for two cases: a finite (F) line, as in Fig. 2, and a semi-infinite (SI) line where $L \to \infty$. The solutions are:

$$\sigma_{SI}(0,t) = 2G\sqrt{\frac{\kappa t}{\pi}} \tag{8}$$

$$\sigma_F(0,t) = GL\left(\frac{1}{2} - 4\sum_{i=0}^{\infty}\frac{e^{-m_i^2(\kappa t/L^2)}}{m_i^2}\right) \tag{9}$$

where $m_i = (2i+1)\pi$. The solution to the SI case is provably an upper bound for the F case: intuitively, this is because the back-stress is lower when the anode is at ∞, which leads to a larger net stress at the cathode. As illustrated in Fig. 3, the two curves closely track each other initially and diverge as t increases. This is explained by the observation in [18] that the steady state for a line of length, L, can be achieved in time $t \approx \frac{L^2}{4\kappa}$. The F and SI curves differ significantly at this time, but are close for smaller values of t, before sufficient back-stress is built up. For long wires (e.g., in power grids in upper level metals), the SI approximation is accurate.

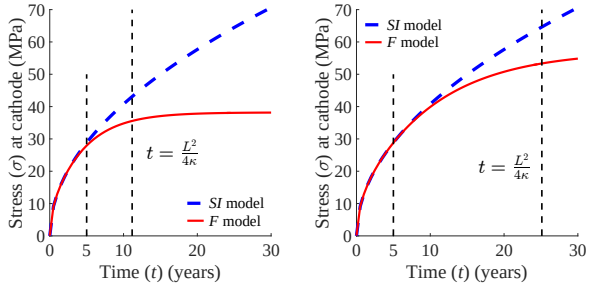

Figure 3: Stress $\sigma(0, t)$ at the cathode for (a) $L = 50\mu$m and (b) $L = 75\mu$m, as predicted by SI and F model for two values of L.

The approach in [27] successively identifies EM-safe wires using three successive filters, where earlier filters are computationally cheaper, and typically capable of filtering out more wires:

Filter 1 uses the Blech criterion to identify immortal wires. This eliminates the largest number of wires that are short and/or have low j.

Filter 2 uses the SI formula (8) to identify whether $\sigma_{SI}(0, t_{life}) < \sigma_{crit}$ where t_{life} is the chip lifetime; since σ_F is upper-bounded by σ_{SI}, this implies that these wires will not nucleate during the lifetime of the chip.

Filter 3 uses the most computationally expensive analysis, to verify whether the remaining wires are EM-safe. This finds a Newton-Raphson solution of the equation $\sigma_F(0, t_{nuc}) = \sigma_c$, where σ_F is truncated to 20 terms, to compute the nucleation time, t_{nuc}.

This approach is efficient because identifies a large fraction of wires as EM-safe through Filters 1 and 2 in a computationally cheap manner, and only a small fraction of wires require the expensive Newton-Raphson computation. This can be extended to capture the statistical nature of EM through the statistical nature of effective diffusivity [24], as in [26, 28].

2.5 Flux divergence in multisegment nets

Fundamentally, EM is induced by divergence of atomic flux, which is typically highest at sites such as vias, contacts, or points where the leads merge. Much of the analysis above is presented for two-terminal lines in a single layer, but real interconnects often have multiple branches, segments, metal layers, and fanouts. For Cu DD interconnect, each change of metal layer constitutes a barrier to

the migration of atoms, resulting in localized effects and boundary conditions that require solutions to Korhonen's equation.

Further, it has been reported in literature that even if the incoming atomic flux (signified by high current density) is high at such sites, the site itself may not fail due to low atomic flux divergence, but a simple, individual-lead based Black's equation continues to predict failure for such a structure. This inefficiency has been recently revisited by various researchers resulting into evolution of alternative paradigms in EM checking [1, 7, 10, 31, 36]. Such alternative methods rely on computing some form of atomic flux divergence at EM-probable sites and subsequently comparing them against set thresholds.

One computationally simple method, reported in [31], is the vector via-node based method, wherein the physical and directional interactions amongst various leads are incorporated to perform the reliability verification. Notably, however, the fundamental inputs required to perform these calculations still remain the individual current density in every single interconnect of the circuit, along with additional information like the circuit topology.

2.6 Signal EM

The preceding approaches assume a current density j in a wire, which is appropriate for power grid wires that largely have a unidirectional current flow. Currents in signal wires flow in both directions, and the reversal of direction leads to some damage recovery. To model this, we define an effective j as:

$$j = j^{+}_{avg} - \mathcal{R} j^{-}_{avg} \tag{10}$$

where $\mathcal{R}$ is an empirical recovery factor for EM (typically 0.7–0.95), and j^{+}_{avg} and j^{-}_{avg} indicate the average current density in each of the two directions. There is some controversy as to whether EM recovery is significant or not, or whether a value of $\mathcal{R} \approx 1$ can be used. Even for $\mathcal{R} = 1$, it should be noted that if the PMOS and NMOS strengths driving a signal line are different, then $|j^{+}_{avg}| \neq |j^{-}_{avg}|$, and the value of j is nonzero.

3 EM IN NANOSCALE TECHNOLOGIES

3.1 Thermally-induced EM acceleration

Designs at advanced nodes are based on FinFETs that provide improved electrostatic control over the channel. These device topologies help reduce short channel effects, increase the drive current, enable the use of lower supply voltages, and provide superior scalability, but also suffer from significant self-heating (SH) issues. The high transistor density results in high heat flux, and inefficient heat-removal paths to the thermal ambient. The thermal conductivity in the confined region of the fin is degraded due to lattice vibrations (phonons), and the addition of buried oxide (BOX) in SOI FinFETs, or the oxide that surrounds nanowires in gate all-around FETs (GAAFETs), further degrades the thermal conduction path [8].

Figs. 4(a)–(c) show the heat transfer paths in a bulk FinFET, an SOI FinFET, and a lateral GAAFET, and Figs. 4(d)–(f) illustrate the cross-sectional thermal profiles due to SH for an array of three fins and two gates, in series, of a cell from a FinFET library. The bulk FinFET, which has the easiest path to thermal ground through the substrate, has the lowest temperatures, followed by the SOI FinFET, where the bulk path is impeded by BOX, and then the GAAFET,

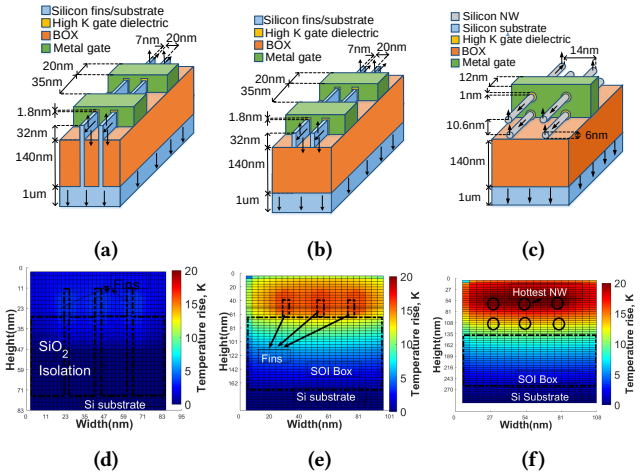

Figure 4: Structure and the paths of heat dissipation in (a) 7nm bulk FinFET, (b) 7nm SOI FinFET, and (c) 5nm lateral GAAFET with arrows that indicate the paths to thermal ground, and thermal contours under a power dissipation of 0.1μW for (d) a bulk FinFET with 3 fins/2 gates (e) an SOI FinFET with 3 fins/2 gates (f) a lateral GAAFET with 3 NW stacks/2 gates.

where thermal paths must negotiate both BOX and the oxide around the NWs, and more heat is conducted through the interconnects. In all these structures, SH can accelerate EM.

In [8], thermal analysis is performed on a set of benchmark circuits. Temperature distributions from thermal analysis are used to estimate the impact on EM using Black's law, and the percentage EM lifetime degradation due to SH is shown in Fig. 5. Degradations in SOI and GAAFET technologies are particularly large, so that wider wires must be used for non-Blech interconnects in these technologies to be EM-safe.

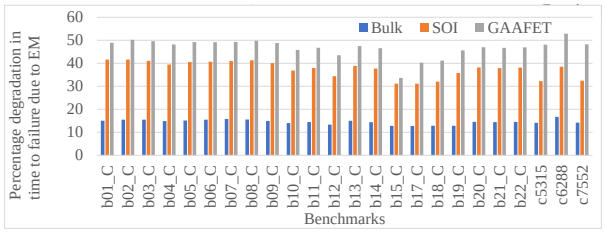

Figure 5: EM-induced time to failure, on benchmark circuits for bulk FinFETs, SOI FinFETs, and GAAFETs.

3.2 EM in lower metal layers

Due to high heat flux and/or high current densities driven in advanced designs, EM can be much more of a problem even in lower metal layers. For instance, cell-internal EM is expressed in signal and power lines within standard cells with high current densities [15, 16, 32, 33]. The signal and power lines could be connected to global interconnects, and thus are not filtered out by the Blech criterion. Similarly, EM may be seen in lower-level metals, an effect that is exacerbated by thermal effects.

The problem of cell-internal EM is illustrated using the INV_X4 (inverter with size 4) cell, shown in Fig. 6(a), from a 45nm library. The input signal A is connected to the polysilicon structure. The layout uses four parallel transistors for the pull-up (poly over p-diffusion, upper half of the figure) and four for the pull-down (poly over n-diffusion, lower half of the figure), and the output signal can be tapped along the H-shaped metal net in the center of the cell. The positions where the output pin can be placed are numbered 1 through 7, and the edges of the structure are labeled e_1 through e_6, as shown in the figure. Since the four PMOS transistors are all identical, by symmetry, the currents injected at nodes 1 and 5 are equal; similarly, the NMOS currents at nodes 3 and 7 are equal.

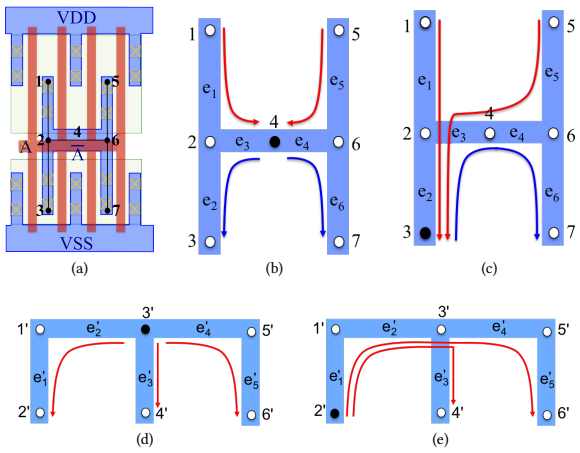

Figure 6: (a) The layout and output pin position options for INV_X4. Charge/discharge currents when the output pin is at (b) node 4 and (c) node 3. The red [blue] lines represent rise [fall] currents. (d) The Vdd pin position options for INV_X4 and the currents when the Vdd pin is at node 3′ and (e) node 2′.

For signal EM, depending on whether the pin is at node 4 (Fig. 6(b)) or node 3 (Fig. 6(c)), the current distribution through the wires within the cell is different. In [32, 33], based on exact parasitic extraction of the layout, fed to SPICE (thus including short-circuit and leakage currents), the average effective EM current through e_2 is found to be 1.17× larger than when the pin is at node 4. Accounting for Joule heating, this results in a 19% lifetime reduction. For the Vdd pin (and similarly for Vss pins), a similar effect occurs when the pin position is changed, as shown in Figs. 6(d) and (e).

3.3 EM in analog circuits

EM is becoming an increasing concern not just in digital circuits, but also in analog designs. Many fundamental analog components carry large currents for long periods of time, e.g., a standard structure is a differential pair connected to a current mirror. Unlike signal wires in digital circuits, these "signal" wires carry unidirectional currents. When coupled with narrowing interconnects in advanced process generations, this implies that the wires connected to these components, even in low metal layers, correspond to a significant current density. This requires the use of wider wires to meet EM lifetime constraints, and this poses a significant issue in analog layout, whereby wire widths must be set based on current densities.

4 ANALYSIS OF INTERCONNECT SYSTEMS

4.1 The weakest link model

A typical EM failure criterion for a wire is a resistance increase of 10%. To translate wire failure to system failure, the weakest link model [9, 20] has been widely used for EM analysis. This is based on the idea that a chip fails on the first EM event, i.e., the chip-level EM failure probability corresponds to the case where no wire experiences EM. At time t, if the failure probability of the i^{th} of K elements is $F_i(t)$, then the probability, $F_{chip}(t)$, of chip failure is:

$$F_{chip}(t) = 1 - \Pi_{i=1}^{K}(1 - F_i(t)) \tag{11}$$

Variations of this approach have been extensively used for on-chip EM analysis [20], but they are largely dependent on making the method simple to use by decoupling the failure of each element from that of other elements. This allows a separate maximum current density check on every wire in the system. However, in many instances, a circuit has inherent resilience that permits it to continue functioning even after an EM event. Fundamentally, the concept of redundancy is a reliability engineer's friend as it enables such resilience. For example, while a tree-structured interconnect may become nonfunctional due to a EM-induced wire break, connectivity in a mesh structure will be maintained even after the first EM failure. In this section, we will first analytically examine the impact of EM failure on system failure, and then provide several examples where the weakest link assumption is invalid.

4.2 Reliability under changing stress

In an interconnect system with redundancy, when one component fails, the current is redistributed to the other wires. This results in higher current densities, and therefore, increases the risk of EM failure in those wires. In this section, we provide a mathematical treatment of this scenario, based on the work in [17].

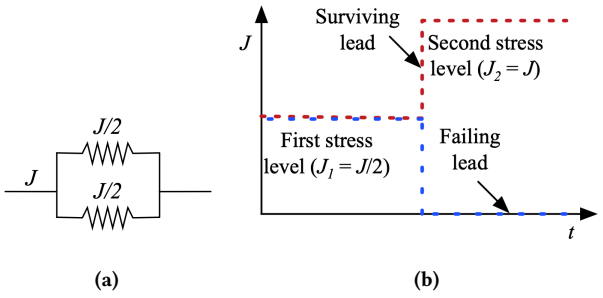

Figure 7: (a) Schematic showing a parallel two-component system (b) Current profile evolution, with first failure occurring at time t1.

Consider a system comprising two components (Fig. 7(a)), where both components initially carry a current density $J_1 = J/2$ (Fig. 7(b)). When one of them fails at time t_1, the current in the surviving component changes to $J_2 = J$. After the first component fails, the current

through the second component rises, altering its failure statistics. The initial failure rate, $f(t)$, of each component is lognormal,

$$f(t) = \frac{1}{t\sigma\sqrt{2\pi}} e^{\left(-\frac{1}{2}\left(\frac{\ln t - \ln t_{50}}{\sigma}\right)\right)} \tag{12}$$

with a cumulative probability distribution function (CDF) given by

$$F(t) = \Phi\left(\frac{\ln t - \ln t_{50}}{\sigma}\right) \tag{13}$$

where $\Phi(x)$ as the standard normal CDF. Until time t_1, the reliability CDF of each component is described by

$$F_1(t) = \Phi\left(\frac{\ln t - \ln t_{50,1}}{\sigma}\right) \tag{14}$$

where $t_{50,1}$ is the mean time to failure for J_1, as in Fig. 8. For a general component that carries current corresponding to second stress level, J_2, the reliability is represented by a CDF, $F_2(t)$, and the associated $t_{50,2}$. For the case of Fig. 7(b), the CDF trajectory for the surviving component at t_1 therefore must change from F_1 to F_2. After the step jump in the current, we shift F_2 by time δ_1 to ensure continuity with F_1 at time t_1, i.e.,

$$F_2(t_1 - \delta_1) = F_1(t_1) \tag{15}$$

This equivalence implies that the curve follows the trajectory of F_2, starting at the same fraction of the failed population under the two stresses, but that the failure rate increases after t_1. For example, for a ξ_{ij} fail probability, shown in Fig. 8, the TTF changes from t_{ijh} (if only the first stress were applicable) to a lower value, t_{ijk} (under the new stress condition). The effective CDF curve (Fig. 8) is

$$F_1(t) = \Phi\left(\frac{\ln t - \ln t_{50,1}}{\sigma}\right) \; 0 \le t \le t_1 \tag{16}$$

$$F_2(t - \delta_1) = \Phi\left(\frac{\ln(t - \delta_1) - \ln t_{50,2}}{\sigma}\right) \; t \ge t_1 \tag{17}$$

$$\text{where} \quad \delta_1 = t_1\left(1 - \frac{t_{50,2}}{t_{50,1}}\right) \tag{18}$$

For a system where components undergo a change in stress multiple times, we can generalize the formulation to account for k changes in current, from J_1 to $J_2 \cdots$ to J_k:

$$\delta_k = \left(t_k - \sum_{i=1}^{k-1} \delta_i\right)\left(1 - \frac{t_{50,k}}{t_{50,k-1}}\right) \tag{19}$$

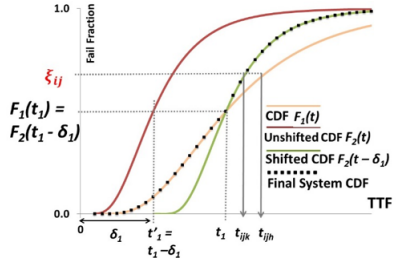

Figure 8: Analytically estimated CDF evolution of a single component when it undergoes a stress change. The dotted line is the effective CDF, when stress change occurs at t_1.

We now apply this idea and basic formulation to analyze the system reliability for the structure in Fig. 7(a). We define the system to be functional as long as there is a valid electrical connection between the two terminals of the parallel system. If both components are from the same process population (Fig. 7(b)), the reliability of the case when both are simultaneously functional is given by:

$$R_{11}(t) = (1 - F_1(t))^2 \tag{20}$$

Next, the reliability for the case when the first component fails at an arbitrary time t_1, and the second component works successfully till time t, is computed. The probability that the first component fails between time t_1 and $(t_1 + \Delta t_1)$ is $f_1(t_1)\Delta t_1$, where $f_1(t)$ is the probability density function associated with $F_1(t)$. After the current redistribution at t_1, the failure statistics of the surviving component are given by the CDF $F_2(t - \delta_1)$. Thus, the probability of the second component working when the first has failed is:

$$[1 - F_2(t - \delta_1)] f_1(t_1)\Delta t_1. \tag{21}$$

Integrating over all possible failure times from 0 to t, the reliability for this case at time t is:

$$R_{12}(t) = \int_{t_1=0}^{t_1=t} [1 - F_2(t - \delta_1)] f_1(t_1) dt_1 \tag{22}$$

The effective failure probability of the parallel configuration is:

$$F_{||}(t) = 1 - [R_{11}(t) + 2R_{12}(t)] \tag{23}$$

For this two-component system, another alternative is to use a single component of twice the width to carry the entire current, $2J_1 = J$. Such a component has the same current density as each of the parallel leads and its failure probability is the single component CDF, F_1, in Fig. 8, which is significantly worse. This margin arises from EM stochasticity, since the probability of two narrower wires failing simultaneously is smaller than that for a single wide wire.

4.3 Power grid IR drop analysis

The power grid is designed as a mesh so that there are multiple paths from the supply/ground pins to any gate. This naturally implies redundancy: even with the loss of a wire segment due to EM failure, there are other current paths to a gate. As in Section 4.2, when a wire fails, the currents to the gate are redistributed along these other paths. While this creates larger EM stress on the wires on these paths, the circuit often functions well after the first failure.

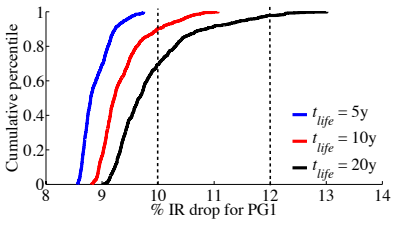

Figure 9: CDF plots for IR drop of the benchmark PG1 for different circuit lifetimes, t_{life}.

The work in [26, 28] presents an analysis of the impact of EM, using probabilistic physics-based models, on the performance of a power grid. Results are shown on the IBM power grid benchmarks, and the cumulative distribution function of the IR drop for PG1 is shown in Fig. 9. It is seen here that as the life of the chip (t_{life}) is increased in simulation, the curves shift to the right, indicating a larger probability of failing an IR drop constraint. The scenarios where the IR drop crosses a threshold are found to correspond to multiple EM failures, rather than a weakest-link failure. The worst-case resistance increase on any wire for the 10- and 20-year lifetime plots is found to be 124% and 297%; in contrast, recall that the basic weakest-link model may pessimistically pronounce system failure when wire resistance increases by 10%.

4.4 Via arrays and thermomechanical stress

Metal lines in the upper metal layers may use wires as wide as 2–3μm, and interconnections between metal layers involve an array of vias instead of a single via. These via arrays have complex geometrical and electrical characteristics that can affect EM, and also contain inherent redundancy as the failure of one via of the array does not imply an open circuit between the connected wires.

Since thermomechanical stress is a function of the layout and the composition of the surrounding layers, the stress in via arrays is position-dependent: vias on the edge of the array see a different CTE environment as compared to vias in the interior. As a result, the critical stress due to EM that causes nucleation is different for vias in the array. This section summarizes the work in [25].

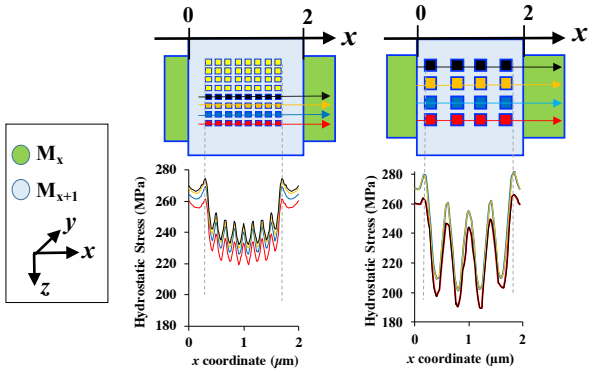

Figure 10: FEA simulation 8×8 vs. 4×4 via array.

Fig. 10 shows two via configurations, corresponding to an 8×8 via array, and another to a 4×4 via array same effective cross section area. The vias connect an upper level of metal M_{x+1} with the next lower level, M_x, and the metal layer heights correspond to M7 and M8 in a 32nm technology node. The wire widths are chosen as 2μm for the interconnects, and are representative of wires in a power grid. Both vias have an effective area of $1\mu m^2$, corresponding to the same resistance between M_x and M_{x+1}.

The figure also shows the results of a finite element analysis (FEA) simulation of the thermomechanical stress through each via. The four curves (black, yellow, green, and red) in each figure represent the hydrostatic stress as a function of distance x, along an arrow of the same color in the figure above. The local minima of stress occur in the interior of each via, and the local maxima occur in the regions between the vias. The stress profile is different for the two scenarios, and although the largest stress in two cases is similar, the inner vias see different stresses.

Current-induced EM stress adds to this residual stress, and voids are formed when the net stress reaches a threshold value [13, 18]. The lower preexisting thermomechanical stress values in the inner vias result in a lower likelihood of achieving the critical threshold value needed for void formation. Moreover, for the 4×4 via array, even if a void does form, its impact may be mitigated by the fact that the via array has more redundancy than a single via. Together, these two factors imply that the choice of the via array dimension can alter interconnect lifetimes.

It is shown in [25] that the thermomechanical stress differences lead to significant lifetime differences for various vias. Additionally, the invalidity of the weakest-link approximation is quite visible in a via array that has a large degree of redundancy. For a 4×4 via ($n = 16$), the failure of one via ($n_F = 1$) results in a 6.7% resistance change, and the failure of eight vias will result in a 100% increase.

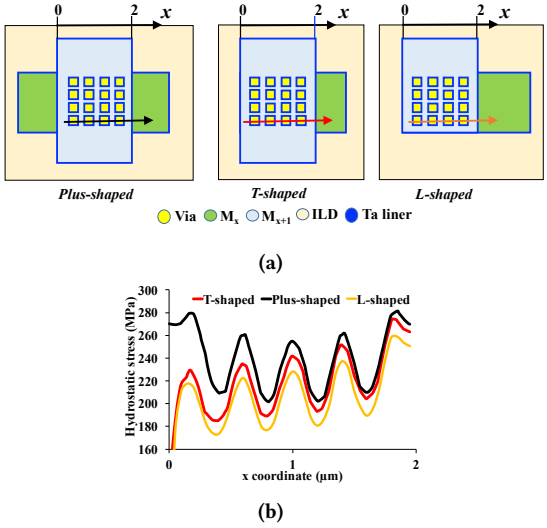

Figure 11: (a) The plus-shaped (left), T-shaped (centre), and L-shaped (right) patterns, illustrated with a 4×4 via array. (b) Thermal stress for these intersection patterns.

The level of thermomechanical stress depends on other factors. For an M_x–M_{x+1} metal layer pair, where x and x+1 may be either intermediate or top layers [2] (with three combinations: intermediate–intermediate, intermediate–top, and top–top), an interconnect in a power grid consists of three patterns of via array structures, corresponding to the structure of the wires in the two metal layers: *Plus-shaped* patterns, *T-shaped* patterns, and *L-shaped* patterns. These patterns are illustrated in Fig. 11(a). Fig. 11(b) shows the thermomechanical stress under the first row of vias (indicated by the arrows in figure above) in the M_x metal layer of a 4×4 via array for each of these patterns. The difference in stress due to the structure of each pattern can be attributed to a larger CTE for Cu relative to ILD: in these cases, the amount of ILD near the via changes the magnitude of CTE mismatch.

4.5 Clock distribution networks

Signal interconnects can be affected by EM over the chip lifetime, subject to the notion of recovery described in Section 2.6. In particular, EM concerns in wires in clock networks, which carry high amounts of current, can be a serious concern. Therefore, much of the chip-level signal EM analysis is focused on ensuring safety of clock nets, even though they are physically routed at non-default widths due to delay considerations. Mesh-structured clock networks [4, 34, 35] are used because of their robustness to clock skew, but they are also inherently resilient to EM due to the presence of multiple paths to each sink node, and multiple driving buffers that are inserted to maintain clock system performance. Due to this redundancy, the clock skew and slew rate can remain robust after some failures in the grid, and a weakest link approach is pessimistic.

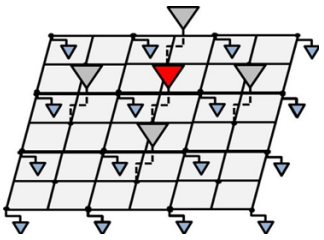

Figure 12: A one-level clock grid schematic with multiple drivers.

These factors were studied in [17] using a Monte Carlo analysis built upon the techniques of Section 4.2. The work considers a one-level clock grid (Fig. 12), with an exemplary buffer and its four identical neighbors to the north, south, east, and west, implemented in a commercial 28nm node, at 1GHz. In our example, wire widths in the clock grid are large so that the likelihood of EM failure is negligible and we focus on failures that may occur in within-cell wires [32] that drive large external wires, or in the power grid. It is shown (Fig. 13) that the weakest link approximation (WLA) significantly underestimates failure, and using a skew-based criterion instead of the WLA results in a ~ 2× lifetime improvement.

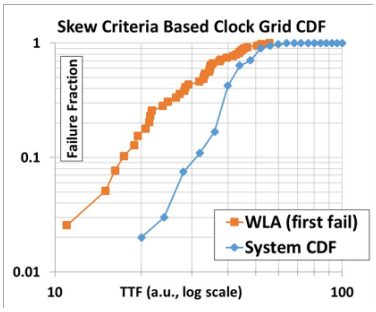

Figure 13: The CDF of lifetime using skew-based criteria based CDF, as against the weakest link approximation (WLA) on a clock grid shows the high level of pessimism of the latter.

5 CONCLUSION

EM is an increasingly significant problem in nanometer-scale designs. The primary message of this paper is that reliable interconnect design requires an understanding not only of the physics that drives EM, but also circuit-level insights into the impact of EM on performance, and scenarios that cause circuits to fail due to EM.

ACKNOWLEDGMENTS

This work was supported in part by the NSF under awards CCF-1421606, CCF-1714805, and by the DARPA IDEA program. The author gratefully acknowledges the work of Dr. Vivek Mishra, Dr. Palkesh Jain, and Vidya Chhabria that led to many of the insights in this paper.

REFERENCES

[1] S. M. Alam, C. L. Gan, F. L. Wei, C. V. Thompson, and D. Troxel. 2005. Circuit-level reliability requirements for Cu metallization. *IEEE T. Device Mater. Rel.* 5, 3 (2005), 522–531.
[2] C. J. Alpert, Z. Li, M. Moffitt, G.-J. Nam, J. Roy, and G. Tellez. 2010. What makes a design difficult to route?. In *Proc. ISPD*. ACM, New York, NY, 7–12.
[3] JEDEC Solid State Technology Association. 2018. Foundry process qualification guidelines (Wafer fabrication manufacturing sites) – Backend of line. JEP001-1A.
[4] D. W. Bailey and B. J. Benschneider. 1998. Clocking design and analysis for a 600-MHz alpha microprocessor. *IEEE J. Solid-St. Circ.* 3, 11 (Nov. 1998), 1627–1633.
[5] J. R. Black. 1969. Electromigration failure modes in aluminum metallization for semiconductor devices. *Proc. IEEE* 57, 9 (1969), 1587–1594.
[6] I. A. Blech. 1976. Electromigration in thin aluminum films on titanium nitride. *J. Appl. Phys.* 47, 4 (1976), 1203–1208.
[7] S. Chatterjee, V. Sukharev, and F. N. Najm. 2018. Power grid electromigration checking using physics-based models. *IEEE T. Comput. Aid D.* 37, 7 (July 2018), 1317–1330.
[8] V. Chhabria and S. S. Sapatnekar. 2019. Impact of self-heating on performance and reliability in FinFET and GAAFET designs. In *Proc. ISQED*. IEEE, Piscataway, NJ.
[9] D. F. Frost and K. F. Poole. 1989. Reliant: a reliability analysis tool for VLSI interconnect. *IEEE J. Solid-St. Circ.* 24, 2 (April 1989), 458–462.
[10] Z. Guan, M. Marek-Sadowska, S. Nassif, and B. Li. 2014. Atomic flux divergence based current conversion scheme for signal line electromigration reliability assessment. In *Proc. IEEE International Interconnect Technology Conference*. IEEE, Piscataway, NJ, 245–248.
[11] J. E. Hall, D. E. Hocevar, Ping Yang, and M. J. McGraw. 1987. SPIDER – A CAD system for modeling VLSI metallization patterns. *IEEE T. Comput. Aid D.* 6, 6 (Nov. 1987), 1023–1031.
[12] C. S. Hau-Riege, S. P. Hau-Riege, and A. P. Marathe. 2004. The effect of interlevel dielectric on the critical tensile stress to void nucleation for the reliability of Cu interconnects. *J. Appl. Phys.* 96, 10 (2004), 5792–5796.
[13] A. Heryanto, K. L. Pey, Y. K. Lim, W. Liu, N. Raghavan, J. Wei, C. L. Gan, M. K. Lim, and J. B. Tan. 2011. The effect of stress migration on electromigration in dual damascene copper interconnects. *J. Appl. Phys.* 109, 1 (2011), 013716–1–013716–9.
[14] W. Hunter. 1997. Self-consistent solutions for allowed interconnect current density. II. Application to design guidelines. *IEEE Transactions on Electron Devices* 44, 2 (Feb. 1997), 310–316.
[15] P. Jain, J. Cortadella, and S. S. Sapatnekar. 2016. A fast and retargetable framework for logic-IP-internal electromigration assessment comprehending advanced waveform effects. *IEEE T. VLSI Syst* 24, 6 (June 2016), 2345–2358.
[16] P. Jain and A. Jain. 2012. Accurate current estimation for interconnect reliability analysis. *IEEE T. VLSI Syst* 20, 9 (Sept. 2012), 1634–1644.
[17] P. Jain, S. S. Sapatnekar, and J. Cortadella. 2015. Stochastic and topologically aware electromigration analysis for clock skew. In *Proc. IRPS*. IEEE, Piscataway, NJ, 3.D.4–1–3.D.4–6.
[18] M. A Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li. 1993. Stress evolution due to electromigration in confined metal lines. *J. Appl. Phys.* 73, 8 (1993), 3790–3799.
[19] K.-D. Lee. 2012. Electromigration recovery and short lead effect under bipolar- and unipolar-pulse current. In *Proc. IRPS*. IEEE, Piscataway, NJ, 6B.3.1–6B.3.4.
[20] B. Li, P. S. McLaughlin, J. P. Bickford, P.Habitz, D. Netrabile, and T. D. Sullivan. 2011. Statistical evaluation of electromigration reliability at chip level. *IEEE T. Device Mater. Rel.* 11, 1 (March 2011), 86–91.
[21] J. Lienig. 2013. Electromigration and its impact on physical design in future technologies. In *Proc. ISPD*. ACM, New York, NY, 33–40.
[22] J. Lienig and M. Thiele. 2018. The pressing need for electromigration-aware physical design. In *Proc. ISPD*. ACM, New York, NY, 144–151.
[23] J.R. Lloyd. 2007. Black's law revisted—Nucleation and growth in electromigration failure. *Microelectron. Reliab.* 47, 9 (2007), 1468–1472.
[24] J. R. Lloyd and J. Kitchin. 1991. The electromigration failure distribution: The fine-line case. *J. Appl. Phys.* 69, 4 (1991), 2117–2127.
[25] V. Mishra, P. Jain, S. K. Marella, and S. S. Sapatnekar. 2016. Incorporating the role of stress on electromigration in power grids with via arrays. In *Proc. DAC*. ACM, New York, NY, 21:1–21:6.
[26] V. Mishra and S. S. Sapatnekar. 2013. The impact of electromigration in copper interconnects on power grid integrity. In *Proc. DAC*. ACM, New York, NY, 88:1–88:6.
[27] V. Mishra and S. S. Sapatnekar. 2016. Predicting electromigration mortality under temperature and product lifetime specifications. In *Proc. DAC*. ACM, New York, NY, 43:1–43:6.
[28] V. Mishra and S. S. Sapatnekar. 2017. Probabilistic wire resistance degradation due to electromigration in i power grids. *IEEE T. Comput. Aid D.* 36, 4 (April 2017), 628–640.
[29] A. S. Oates. 2015. Strategies to ensure electromigration reliability of Cu/Low-k interconnects at 10 nm. *ECS J. Solid State Sc. Tech.* 4, 1 (2015), N3168–N3176.
[30] J.-M. Paik, H. Park, and Y.-C. Joo. 2004. Effect of low-k dielectric on stress and stress-induced damage in Cu interconnects. *Microelectron. Eng.* 71, 3–4 (2004), 348–357.
[31] Y. J. Park, P. Jain, and S. Krishnan. 2010. New electromigration validation: Via node vector method. In *Proc. IRPS*. IEEE, Piscataway, NJ, 698–704.
[32] G. Posser, V. Mishra, P. Jain, R. Reis, and S. S. Sapatnekar. 2014. A systematic approach for analyzing and optimizing cell-internal signal electromigration. In *Proc. ICCAD*. IEEE, Piscataway, NJ, 486–491.
[33] G. Posser, V. Mishra, P. Jain, R. Reis, and S. S. Sapatnekar. 2016. Cell-internal electromigration: Analysis and pin placement based optimization. *IEEE T. Comput. Aid D.* 35, 2 (Feb. 2016), 220–231.
[34] H. Qian et al. 2012. Subtractive router for tree-driven-grid clocks. *IEEE T. Comput. Aid D.* 31, 6 (June 2012), 868–877.
[35] H. Su and S. S. Sapatnekar. 2001. Hybrid structured clock network construction. In *Proc. ICCAD*. IEEE, Piscataway, NJ, 333–336.
[36] Z. Sun, E. Demircan, M. D. Shroff, C. Cook, and S. X.-D. Tan. 2018. Fast electromigration immortality analysis for multisegment copper interconnect wires. *IEEE T. Comput. Aid D.* 37, 12 (Dec. 2018), 3137–3150.
[37] C.-C. Teng, Y.-K. Cheng, E. Rosenbaum, and S.-M. Kang. 1997. iTEM: A temperature-dependent electromigration reliability diagnosis tool. *IEEE T. Comput. Aid D.* 16, 8 (Aug. 1997), 882–893.
[38] L. M. Ting, J. S. May, W. R. Hunter, and J. W. McPherson. 1993. AC electromigration characterization and modeling of multilayered interconnects. In *Proc. IRPS*. IEEE, Piscataway, NJ, 311–316.