Understanding the Impact of Transistor-Level BTI Variability

Jianxin Fang and Sachin S. Sapatnekar
Department of Electrical and Computer Engineering, University of Minnesota,
200 Union Street SE, Minneapolis, MN 55455.

***Abstract*—Recent work has shown large variations due to bias-temperature instability (BTI) at the device level, and we study its impact on the behavior of larger circuits. We propose an analytical method that is over 600x faster than Monte Carlo simulation and accurate for technologies down to 16nm, and demonstrate it on circuits with up to 68,000 transistors. Results show that the impact of BTI variability at the circuit level is significantly smaller than at the device level, but increases with device downscaling.**

Keywords-Bias-Temperature Instability (BTI); Variability; Digital Circuit Delay; Degradation Analysis

I. INTRODUCTION

Bias temperature instability (BTI) is a major reliability concern in deeply-scaled very large scale integrated (VLSI) circuits. The BTI effect causes the threshold voltage, V_{th}, of CMOS transistors to increase under voltage tress, resulting in a temporally-dependent degradation in the signal propagation delay in digital circuits.

The reaction-diffusion (R-D) model [1] for BTI, based on the dissociation of Si–H bonds at the Si/SiO_2 interface, has been a prevailing theory of the mechanism of BTI, and has been widely employed in research on circuit reliability and optimization. However, over the years, several limitations in the R-D theory have been exposed. For example, the predictions from R-D theory are unable to adequately explain the experimentally observed sensitivity of the degradation to the applied gate bias. Moreover, the observed recovery begins faster and lasts longer than that predicted by R-D models. These issues are addressed by recent advances in BTI modeling [2], based on the charge trapping/detrapping theory, in which the temporal $V_{\rm th}$ variations are caused by defects in gate dielectrics that can capture charged carriers.

Moreover, the charge trapping model explains the observation that for small-area devices the degradation and recovery of ΔV_{th} proceed in discrete steps [2], which is similar to the case of random telegraph noise (RTN) and $1/f^2$ noise. Based on the charge trapping model, the intrinsic variability of BTI effect was explored analytically in [3], which indicates the possibility of very large device-level variations for small-geometry FETs, leading to orders-of-magnitude lifetime variations. These models were incorporated in a circuit simulator [4] and demonstrated on an inverter circuit, predicting large delay variations (with σ/μ of over 20%). However the proposed approaches in [4] were based on SPICE-like circuit simulation that feeds a Monte Carlo method, and this approach is not scalable to large-scale digital circuits.

A significant unanswered question, which this paper attempts to address, is: how does this large device-level variation translate to variations at the circuit level? We answer this question by:

(a) taking large circuits in 32nm, 22nm, and 16nm technologies,
(b) mapping them to a standard-cell library to meet realistic timing specifications, and
(c) examining and analyzing the results.

SPICE-based approaches are inefficient in finding the critical paths in large circuits, and hence a cell-based timing model is used in this work, consistent with the approaches used for timing analysis in realistic circuits. An analytical method is proposed for finding the variation in delay on the critical path, and verified using Monte Carlo simulations.

We find that BTI variability increases with downscaling, but that circuit-level variations are significantly lower than device-level variations. After we present our experimental results, we will analyze the reason for this reduction in the magnitude of variations. We also show that this circuit delay variation is Gaussian in nature, and the degradation is proportional to the logarithm of time.

II. MODELING

A. BTI Variability under Charge Trapping Model

As discussed in [4][5], the threshold voltage degradation ΔV_{th} of small-geometry devices shows significant levels of uncertainty due to the random nature of the spatial distribution of defects in the dielectric, as well as the impact on ΔV_{th} of each defect. Under the charge trapping model for BTI, each MOS device is characterized by the number of defects, the capture and emission time of each defect, and the impact on device V_{th} when each defect is charged [4]. These defect parameters are characterized in device experiments for given semiconductor technology using the recently-proposed time-dependent defect spectroscopy (TDDS) method [6].

For a MOS device of length L and width W, the total number of defects is modeled as a Poisson distribution, $n\sim\text{Poisson}(N)$, with mean value $N = N_{ot}WL$, where N_{ot} stands for the dielectric areal defect density . The BTI-induced threshold degradation due to each single defect when charged

(occupied) is modeled as an exponential distribution, $\Delta V_{th} \sim \mathrm{Exp}(\eta)$, with mean value $\eta = \eta_0/WL$ [3]. Both N_{ot} and η_0 are technology-specific parameters.

At any given time, each of the defects in the MOS device has two states: charged (occupied) or uncharged. Only occupied defects make contributions to the device threshold voltage. Following the models in [7], the timing characteristics of each defect corresponding to the charge trapping and detrapping events, namely the capture and emission time τ_c and τ_e, are strongly dependent on voltage and temperature. In digital circuits, the voltage dependence effect is simplified by the fact that there are only two nontransient voltage stages – logic 1 and logic 0 – corresponding to two static modes of stress and relaxation. We capture the temperature dependence effect by the use of a standard corner-based approach where the worst-case temperature corner is assumed. Thus each defect can be described by four time constants, denoted as vector $\boldsymbol{\tau}$,

$$\boldsymbol{\tau} = \left(\tau_{c,\mathrm{Stress}}, \tau_{c,\mathrm{Relax}}, \tau_{e,\mathrm{Stress}}, \tau_{e,\mathrm{Relax}}\right). \quad (1)$$

The trapping and detrapping of electric charges in a defect is a stochastic process with time constants characterized by the vector $\boldsymbol{\tau}$. The occupancy probability (i.e., the probability of charge trapping) of a single defect under AC stress is derived in [7] to be a function of total time t and duty factor DF as follows,

$$P_c(DF, t, \boldsymbol{\tau}) = \frac{\tau_e^*}{\tau_c^* + \tau_e^*}\left(1 - \exp\left(-\left(\frac{1}{\tau_c^*} + \frac{1}{\tau_e^*}\right)\mathrm{t}\right)\right). \quad (2)$$

Here, the duty factor DF of a device under AC stress is defined as the probability of the transistor in accumulation mode that is effective for BTI stressing (in some papers, DF is also referred to as the signal probability, SP). The parameters τ_c^* and τ_e^* are defined as the effective capture and emission time constants under AC stress, which account for the duty factor effect are functions of DF:

$$\frac{1}{\tau_c^*} = \frac{DF}{\tau_{c,\mathrm{Stress}}} + \frac{1 - DF}{\tau_{c,\mathrm{Relax}}} \quad (3)$$

$$\frac{1}{\tau_e^*} = \frac{DF}{\tau_{e,\mathrm{Stress}}} + \frac{1 - DF}{\tau_{e,\mathrm{Relax}}} \quad (4)$$

Fig. 1 shows an example plot of the occupancy probability function $P_c(DF, t, \boldsymbol{\tau})$ of a single defect as defined in (2), with the values of the time constants $\boldsymbol{\tau}$ shown in the figure. The plot indicates that the occupancy probability increases from zero to an asymptotic value of one. It can be seen that as a function of DF, P_c increases gradually. The time over which this change occurs is relatively in a short time compared to the circuit lifetime, which is in the range of 10^5 to 10^6 a.u.

B. The Mean Defect Occupancy Probability

Since the defects are created in the fabrication process and uniformly distributed in the dielectric layer, for each individual component of $\boldsymbol{\tau}$, the statistical distribution associated with any defect in a wafer is independent and identically distributed. The

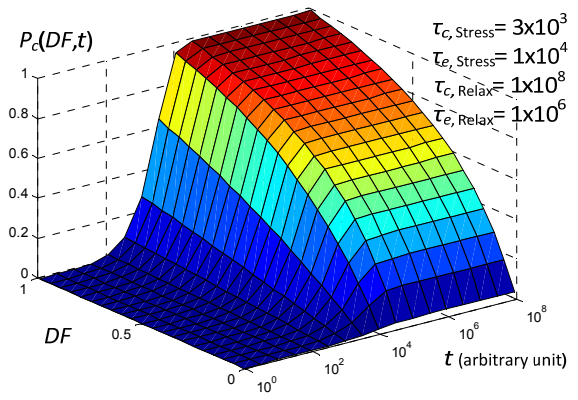

Figure 1. Example of the occupancy probability function of a single defect.

statistical distributions of different time constants in the $\boldsymbol{\tau}$ vector may be different, and for each single defect the four components of $\boldsymbol{\tau}$ are correlated according to [6], and their joint distribution can be characterized for a specific technology. In this paper, we follow the assumptions in [4] and use the following distributions to generate the time constants:

- $\tau_{e,\mathrm{Relax}}$ is uniformly distributed on the log scale between 10^1 and 10^{10}a.u.
- $\tau_{c,\mathrm{Stress}}$ and $\tau_{e,\mathrm{Stress}}$ are also taken to be uniformly distributed on the log scale and weakly correlated with $\tau_{e,\mathrm{Relax}}$ with mean values μ given by $\mu_{\tau_{c,\mathrm{Stress}}} = 0.1\mu_{\tau_{e,\mathrm{Relax}}}$ and $\mu_{\tau_{e,\mathrm{Stress}}} = 100\mu_{\tau_{e,\mathrm{Relax}}}$.
- $\tau_{c,\mathrm{Relax}}$ is assumed to be much larger than the other time constants, and uniformly distributed on the log scale between 10^9 and 10^{15} a.u.

Fig. 2 shows an example 2-D histogram of the joint distribution of $\tau_{c,\mathrm{Stress}}$ and $\tau_{e,\mathrm{Relax}}$, the dominant components of $\boldsymbol{\tau}$.

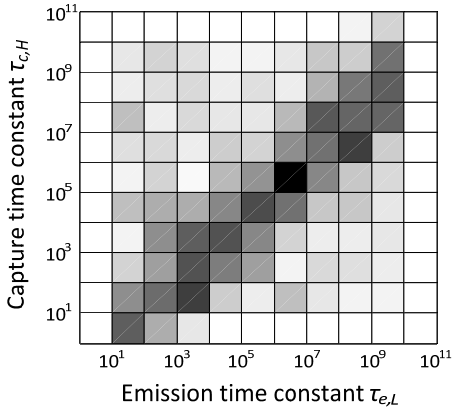

Figure 2. An example of the joint distribution of $\tau_{e,L}$ and $\tau_{c,H}$.

With these assumptions, the mean occupancy probability function, $\overline{P_c}(DF, t)$, is introduced as the expected value of the occupancy probability of a single defect defined in (2):

$$\overline{P_c}(DF, t) = \int P_c(DF, t, \boldsymbol{\tau}) f(\boldsymbol{\tau}) d\boldsymbol{\tau} \quad (5)$$

Here $f(\boldsymbol{\tau})$ is the joint probability distribution function (PDF) of $\boldsymbol{\tau}$. The mean occupancy probability function $\overline{P}_c(DF,t)$ can be calculated by evaluating (5) numerically. Fig. 3 shows the $\overline{P}_c(DF,t)$ function corresponding to the assumed $f(\boldsymbol{\tau})$ that is plotted in Fig. 2. This plot indicates that the mean occupancy probability is a monotonically increasing function of both DF and time. Even though $P_c(DF,t,\boldsymbol{\tau})$ increases rapidly with t for a single defect with a specific $\boldsymbol{\tau}$, as shown in Fig. 1, due to averaging effects of large number of defects with different time constants, $\overline{P}_c(DF,t)$ changes more gradually with time.

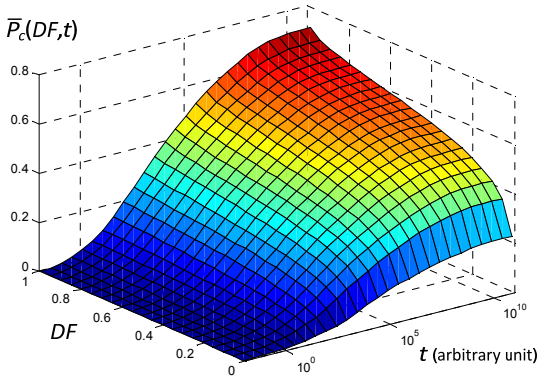

Figure 3. The plot of mean defect occupancy probability function

Since $\overline{P}_c(DF,t)$ is only determined by the distribution $f(\boldsymbol{\tau})$ which is technology-related, and independent of the circuit structure, it can be pre-characterized and stored in a look-up table (LUT) for use in circuit analysis.

C. Cell Delay Model of Digital Circuits

Due to BTI effects, the threshold voltages of stressed increase over time. The propatation delay of a logic cell (e.g., NAND, NOR) in a digital circuit is dependent on the V_{th} of all MOS transistors in the cell, and therefore digital circuits slow down as they age.

Based on a commonly-used model [8], we use a cell delay degradation model based on a first-order Taylor approximation. The delay d_i of cell i is modeled as a linear function of $\Delta V_{th}^{(j)}$ of each transistor j in cell i:

$$d_i = d_{i0} + \sum_{j\in \text{cell } i} \frac{\partial d_i}{\partial V_{th}^{(j)}} \Delta V_{th}^{(j)} = d_{i0} + \sum_{j\in \text{cell } i} S_{ij} \Delta V_{th}^{(j)} \quad (6)$$

Here d_{i0} is the nominal value of delay, $S_{ij} = \partial d_i / \partial V_{th}^{(j)}$ are the sensitivities of delay d_i to the threshold of device j at the nominal threshold voltage. These parameters are calculated using standard design automation techniques, built on top of SPICE simulations.

The characterization of cell delay and sensitivities is also circuit-independent and depends purely on the cell library: hence as part of library characterization, these values are computed for each cell in the library and stored in LUTs.

III. Analysis of Circuit Delay Degradation

The delay of a digital logic circuit is calculated by static timing analysis (STA). The digital circuit is modeled as a directed acyclic graph (DAG). The circuit delay is the sum of the delay of logic cells on the longest signal path, or critical path, as $D = \sum_{i\in \text{critical path}} d_i$, which limits the maximum operation frequency of the digital circuit: $f_{\text{clock}} \le 1/D$. This paper calculates the circuit delay degradation due to BTI based on the critical path. The duty factor DF of each transistor in the circuit is calculated using standard techniques [9].

A. Analytical Method

Based on the mean defect occupancy probability function (5) introduced in Section II.B, the number of occupied defects, denoted as n_c, of a transistor has a Poisson distribution [1] $n_c \sim \text{Poisson}(N_c)$, with its mean value N_c calculated using $\overline{P}_c(DF,t)$.

$$N_c = N \cdot \overline{P}_c(DF,t) = N_{ot} WL \cdot \overline{P}_c(DF,t) \quad (7)$$

The total threshold voltage degradation, ΔV_{th}, of a transistor is the sum of contributions to the degradation from all *occupied* defects in the transistor, i.e.,

$$\Delta V_{th} = \sum_{i=1}^{n_c} \Delta V_{th}^{(i)} \quad (8)$$

Since the $\Delta V_{th}^{(i)}$ values of all defects are independent and identically distributed (i.i.d.) as discussed in Section II.A, the total ΔV_{th} is a sum of n_c exponential random variables, while n_c has a Poisson distribution. A closed form for this sum is found in [3] and both the PDF and CDF of ΔV_{th}.

The distribution functions have complex form, but the probit plot of the CDF function in [3] indicates that for an adequate number of defects (e.g., $N_c \ge 10$), the BTI-drive ΔV_{th} can be approximated as following Gaussian distribution:

$$\Delta V_{th(\text{BTI})} \sim N(\mu, \sigma^2), \quad (9)$$

$$\text{where } \mu = N_c \eta \text{ and } \sigma^2 = 2N_c \eta^2$$

This Gaussian approximation can be justified by the central limit theorem (CLT) for a large number N_c of occupied defects. As shown in Section IV, this approximation does not induce significant errors to the circuit level results.

If process-induced variation of device V_{th} is also considered, which is modeled as an independent Gaussian distribution, $V_{th(\text{proc})} \sim N(V_{th0}, \sigma_0^2)$. The combined V_{th} degradation of MOS transistor j can be expressed as

[1] The number of occupied defects in a device follows a Poisson distribution by definition because (a) each occupied defect has the same occurrence rate $N_c/(WL)$ within the device area of W by L, and (b) the occurrence of all occupied defects are independent with each other. This is similar to the number of all defects which follows $n \sim \text{Poisson}(N)$, and is verified by experiments in Sec IV.

$$\Delta V_{th}^{(j)} \sim N(\mu_j, \sigma_j^2), \tag{10}$$

$$\text{where } \mu_j = N_c\eta \text{ and } \sigma_j^2 = 2N_c\eta^2 + \sigma_0^2$$

In a digital circuit, the critical path is obtained from STA. Based on the cell delay model in (6), the delay degradation of the critical path is derived as

$$D = D_0 + \Delta D = D_0 + \sum_{i \in \text{critical path}} \Delta d_i \tag{11}$$

$$= D_0 + \sum_{i \in \text{critical path}} \sum_{j \in \text{cell } i} S_{ij} \Delta V_{th}^{(j)}$$

Since the $\Delta V_{th}^{(j)}$ of each transistor are independent Gaussian random variables, the degraded delay also has a Gaussian distribution with mean and variance as follows

$$\mu_D = D_0 + \sum_{i \in \text{critical path}} \sum_{j \in \text{cell } i} S_{ij}\mu_j \tag{12}$$

$$\sigma_D^2 = \sum_{i \in \text{critical path}} \sum_{j \in \text{cell } i} S_{ij}^2 \sigma_j^2$$

B. *Monte Carlo Method for Verification*

The Monte Carlo flow for calculating the delay degradation is shown in Fig. 4. This Monte Carlo simulation yields the distribution of delay degradation, and it is employed in this work to verify the proposed analysis method.

INPUT: The critical path of the circuit from initial STA, and the DF of each device
for each Monte Carlo sample of circuit $m = 1,2, \dots, M$
  for each PMOS device j in the circuit, with size $W_j \cdot L_j$
    Generate the initial $V_{thj0} \sim N(V_{th0}, \sigma_0^2)$
    Generate number of defects $n \sim \text{Poisson}(N_{ot} W_j L_j)$
    for each defect $k = 1,2, \dots, n$
      Generate $\boldsymbol{\tau}$ from the distribution, calculate $P_c(DF_j, t)$
      Randomly determine whether defect k is occupied
      if k is occupied, generate $\Delta V_{thk} \sim \text{Exp}(\eta_0 / W_j L_j)$
  Calculate $V_{thj} = V_{\text{th}j0} + \sum_{k \text{ occupied}} \Delta V_{thk}$
  Calculate the critical path delay D_m using (11)

Figure 4. Monte Carlo flow for delay degradation analysis.

C. *Overall Analysis Flow*

As shown in Fig. 5, the flow of the BTI variability analysis procedure is as follows:

- The input is a digital circuit, the corresponding cell library, and the technology parameters.
- The mean defect occupancy probability $\overline{P_c}(DF, t)$ and cell delay sensitivities are characterized offline (Section II.B, II.C). For each circuit, the nominal critical path delay D_0 and DF are computed using EDA techniques.

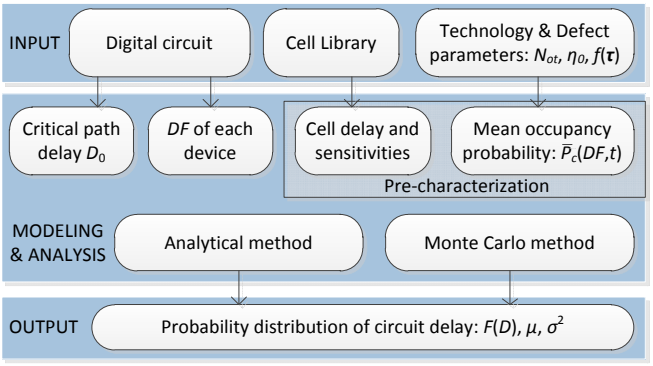

Figure 5. Flow chart of the analysis of BTI variability in digital circuits.

- The analytical (Section III.A) method is used to determine circuit delay degradation and its variation spreads under BTI variability.

When we evaluate the correctness and accuracy of our method, the third step is replaced by the Monte Carlo method (Section III.B). As we will show in the results, the analytical method provides accurate results, and is over 600 times faster than Monte Carlo.

IV. Experimental Results

The proposed approaches for circuit delay degradation analysis under BTI variability are applied to ISCAS85 and ITC99 benchmarks, which are mapped to a subset of the Nangate cell library [10], and scaled down to 32nm, 22nm and 16nm for comparison. The characterization of cell delay and sensitivities is performed using HSPICE with PTM models [11]. Both the analytical and Monte Carlo methods are implemented in C++ and executed on a Linux PC with 3GHz CPU and 2GB RAM.

Table I shows the circuit delay degradation at $t = 10^5$ a.u. at different technology nodes. The mean delay degradation is listed in columns named $\Delta D\%$, while the columns named $\sigma'/\mu\%$ show the normalized standard deviation of circuit delay as a percentage of the mean, for only BTI-induced variation (without including process-induced V_{th0} variation). Next, process-induced V_{th0}variation is added in, setting $\sigma_0/\mu = 5\%$, and we show the results of the corresponding normalized standard deviation of circuit delay, as a percentage of the mean, in the columns labelled $\sigma/\mu\%$. The errors of the proposed method as compared to Monte Carlo (MC) simulation and the runtime comparisons are also shown in the table. On average, the proposed method has 1.31% error in ΔD and 0.76% error in σ, and is over 600× faster compared with MC.

Simulation results in Table I indicate that even with significant device-level variations (the combined σ/μ of V_{th} is up to 4.5% due to both BTI variability and process variation for these experiments). Therefore, the circuit level impact of BTI variability is much less than device level; however it increases with device downscaling, and is more noticeable at 16nm.

The results also verify the proposed analytical method is accurate as compared to Monte Carlo. The probit plot of the delay distributions (analytical and Monte Carlo) of benchmark

TABLE I. MEAN AND RELATIVE STANDARD DEVIATION (WITHOUT AND WITH PROCESS-INDUCED V_{th} VARIATION) OF BENCHMARKS USING PROPOSED ANALYSIS METHOD.

Circuit	#MOS	32nm					22nm					16nm					Runtime (s)	
		Analytical Method			Error to MC%		Analytical Method			Error to MC%		Analytical Method			Error to MC%			
		ΔD%	σ'/μ%	σ/μ%	ΔD	σ	ΔD%	σ'/μ%	σ/μ%	ΔD	σ	ΔD%	σ'/μ%	σ/μ%	ΔD	σ	Analytical	MC
c432	876	17.9	0.97	2.28	0.45	0.86	23.6	1.63	2.70	-1.72	0.70	30.6	2.65	3.51	1.17	0.07	0.06	33.2
c880	1490	15.6	1.08	3.08	-0.49	0.87	14.7	1.29	2.56	1.59	-0.16	16.4	1.89	3.01	0.85	-0.14	0.06	31.7
c1355	2428	31.8	1.04	2.50	-2.54	0.31	30.3	1.58	2.65	0.29	1.33	23.6	2.70	3.40	0.37	0.83	0.07	51.8
c1908	1900	15.2	1.30	2.81	-3.11	-0.94	13.9	1.95	2.69	1.66	0.22	15.0	2.99	3.57	-1.62	-0.79	0.07	33.5
c2670	2956	9.94	1.27	2.52	-1.65	0.48	9.68	1.65	2.58	-1.36	-0.45	12.6	2.43	3.14	0.47	0.01	0.07	38.1
c3540	5084	16.6	1.41	2.67	-0.60	0.87	16.2	1.98	2.75	1.74	1.15	18.1	2.90	3.47	1.28	-0.73	0.07	47.0
c5315	7056	19.5	1.21	2.48	0.58	0.43	22.4	1.62	2.35	-0.36	-0.26	26.1	2.46	3.03	0.37	-0.21	0.08	66.3
c6288	16724	20.7	0.81	1.45	0.95	1.82	17.6	1.05	1.48	-2.21	-0.70	21.2	1.44	1.81	-1.57	0.42	0.10	181.2
c7552	9726	16.6	0.86	1.99	0.46	0.11	19.9	2.01	2.84	-2.13	0.25	24.5	2.97	3.61	1.99	-0.68	0.07	54.0
b14	23608	13.3	0.74	1.91	0.52	-0.38	14.3	2.05	2.89	-0.52	-0.42	18.0	3.21	3.85	1.09	-1.51	0.13	40.3
b15	31338	25.6	1.86	2.85	1.98	-0.97	26.2	2.50	3.19	-2.5	0.25	30.8	3.62	4.15	-2.76	-2.37	0.14	71.4
b17	97858	11.0	1.19	2.28	0.55	-0.23	11.1	1.68	2.43	-2.25	-0.76	15.0	2.48	3.11	-2.64	-0.26	0.30	118.4
b20	51874	15.0	1.30	2.48	-0.08	1.74	16.4	1.93	2.74	1.61	-2.2	17.9	1.68	2.28	0.31	1.46	0.18	72.7
b21	50260	13.2	0.65	1.75	-1.15	0.69	15.8	1.64	2.39	0.45	-0.63	16.3	1.58	2.28	-2.96	-1.9	0.19	64.5
b22	68850	15.4	1.96	2.98	0.01	0.39	15.9	2.77	3.41	0.64	0.47	18.0	4.07	4.53	3.2	-1.72	0.26	105.5
Average Error%		-	-	-	1.01	0.74	-	-	-	1.40	0.66	-	-	-	1.51	0.87	Average	619×

circuit c432 under 32nm, 22nm and 16nm technologies are shown in Fig. 6. The Monte Carlo and the analytical results show near-perfect overlap in each case, indicating the proposed analysis method gives accurate results, and that the circuit delay has a Gaussian distribution.

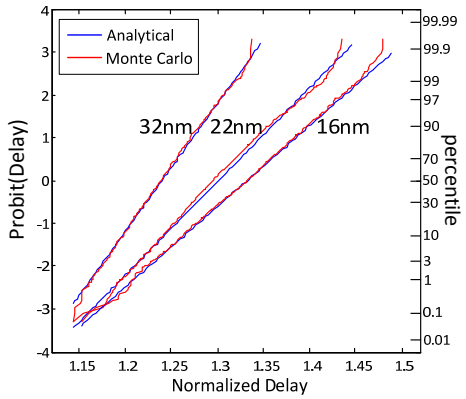

Figure 6. Probit plot of normalized delay distribution of benchmark c432.

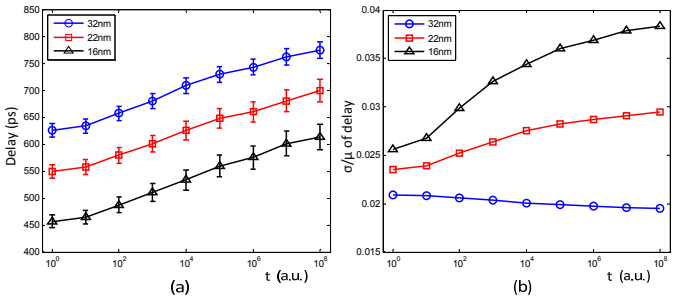

Figure 7. (a) The delay of benchmark c7552 with $\pm\sigma$ error bar vs. time. (b) The corresponding σ/μ of circuit delay vs. time.

Fig. 7 (a) presents the delay degradation versus time with $\pm\sigma$ error bar of c7552. The circuit delay degradation roughly follows the logarithm of time. Both the mean and variance of circuit delay increases with time due to the BTI variability. The ratio σ/μ of circuit delay is plotted in Fig. 7 (b), which increases notably with time for 16nm and 22nm technologies, and decreases slightly with time for 32nm. This result indicates that the transistor-level BTI variability results in a growing impact on circuit-level timing as technology scales down.

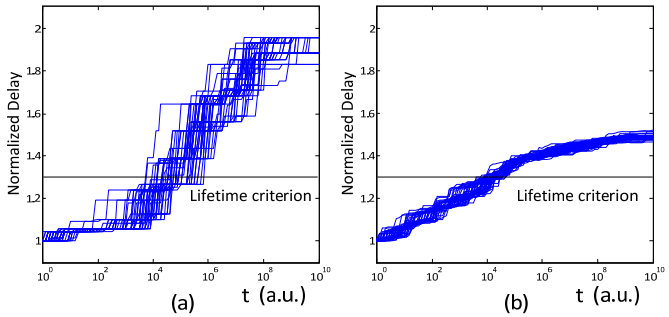

Figure 8. Monte Carlo simulation results of the normalized delay vs. time for inverter chains of (a) one stage and (b) ten stages.

The reduced circuit delay variations can be explained by the following factors.

- First, random variations cancel out over multiple stages on a critical path, as shown in Fig. 8; for a path consisting of N cells with independent variations, the overall variance goes down by $1/\sqrt{N}$, according to central limit theorem (CLT)[2]. Fig. 8 shows the Monte Carlo results of the normalized delay vs. time for inverter chains of (a) one stage and (b) ten stages. The narrower spread of curves in (b) in both x and y direction indicates smaller variations of both lifetime and delay on longer critical path.
- Second, device-level variations are largest for small-geometry FETs. However, devices on critical path in real circuits are sized larger to meet the timing specifications. Smaller FETs are used in off-critical paths, and large delay variations there do not matter since even the altered delays do not exceed the clock period constraint.

[2] The $1/\sqrt{N}$ reduction is a theoretical prediction, and practical results may vary depending on the circuit structure.

V. CONCLUSION

This paper studies the impact of BTI variability on the behavior of larger circuits under charge trapping model. We propose an analytical method for technologies down to 16nm that is fast and confirm its accuracy with Monte Carlo simulations. Our results have shown that although device-level variations can be extremely large in scaled technologies, they result in moderate circuit variations, primarily due to the averaging effect over multiple stages, and the fact that minimum-sized devices are usually not used on critical paths.

REFERENCES

[1] M. A. Alam. "A critical examination of the mechanics of dynamic NBTI for PMOSFETs", Proceedings of the IEEE International Electronic Devices Meeting, pp. 14.4.1–14.4.4, December 2003.

[2] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P.-J. Wagner, F. Schanovsky, J. Franco, P. Roussel, and M. Nelhiebel, "Recent advances in understanding the bias temperature instability", Proceedings of the IEEE International Electronic Devices Meeting, pp. 4.4.1–4.4.4, December 2010.

[3] B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, R. Degraeve, L. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, "Origin of NBTI variability in deeply scaled pFETs", Proceedings of the IEEE International Reliability Physics Symposium, pp. 26–32, May 2010.

[4] B. Kaczer, S. Mahato, V. V. de Almeida Camargo, M. Toledano-Luque, P. J. Roussel, T. Grasser, F. Catthoor, P. Dobrovolny, P. Zuber, G. Wirth, and G. Groeseneken, "Atomistic approach to variability of bias-temperature instability in circuit simulations", Proceedings of the IEEE International Reliability Physics Symposium, pp. XT.3.1–XT.3.5, April 2011.

[5] H. Reisinger, T. Grasser, W. Gustin, and C. Schlünder, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress", Proceedings of the IEEE International Reliability Physics Symposium, pp. 7–15, May 2010.

[6] T. Grasser, H. Reisinger, P.-J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability", Proceedings of the IEEE International Reliability Physics Symposium, pp. 16–25, May 2010.

[7] M. Toledano-Luque, B. Kaczer, P. J. Roussel, T. Grasser, G. I. Wirth, J. Franco, C. Vrancken, N. Horiguchi, and G. Groeseneken, "Response of a single trap to AC negative bias temperature stress", Proceedings of the IEEE International Reliability Physics Symposium, pp. 4A.2.1–4A.2.8, April 2011.

[8] B. C. Paul, K. Kang, H. Kufluoglu, M. A. Alam, and K. Roy, "Impact of NBTI on the temporal performance degradation of digital circuits", IEEE Electron Device Letters, vol. 26, no. 8, pp. 560–562, August 2005.

[9] J. Fang and S. S. Sapatnekar, "Scalable methods for the analysis and optimization of gate oxide breakdown", Proceedings of the IEEE International Symposium on Quality Electronic Design, pp. 638–645, March 2010.

[10] Nangate 45nm Open Cell Library. http://www.si2.org/openeda.si2.org/projects/nangatelib

[11] Predictive Technology Model. http://www.eas.asu.edu/~ptm