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Self-Tiling Monocrystalline Silicon; a Process to Produce Electrically Connected Domains of Si and Microconcentrator Solar Cell Modules on Plastic Supports

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The emerging fields of macro and printable electronics aim to realize large-area-integration of semiconductor devices on curved, flexible, and inexpensive substrates. Current processes to deliver active materials include inkjet printing, parallel transfer, robotic pick-and-place, and fluidic self-assembly. Inkjet printing is most suited to produce low performance organic semiconductors and hybrid organic/inorganic structures, while parallel transfer[1–4] and self-assembly techniques[5–9] target the integration of higher performance inorganic devices that may undergo high temperature processing on flexible, low temperature substrates in a massively parallel fashion. Applications include flexible[10] and curved displays,[8] curved focal plane arrays,[2] oscillators,[3] RFID tags[11] and solar cells[4] incorporating ZnO,[12] GaAs,[7,13] InP,[14] GaN,[15,16] and Si.[2,3,8,17,18] Transfer techniques, when compared to engineered self-assembly methods, use a donor substrate/wafer and maintain orientation and integration density, which is in stark contrast to directed self-assembly,[19] which can redistribute components over large areas and order unorganized parts. For example, a container full of semiconductor dies/chiplets can be redistributed and assembled at precise locations on a substrate at any desired pitch or required functional density using the methods of directed self-assembly. At present, there are two comparable self-assembly methods to assemble semiconductor dies/chiplets with yields approaching 100%. The first method uses gravity in combination with complementary 3D shapes to assemble trapezoidal Si dies onto plastic substrates.[6,20,21] The second uses gravity in combination with surface tension-directed assembly, either using hydrophilic/hydrophobic surface patterns,[22–25] or solder-patterned surfaces to assemble and electrically connect semiconductor dies/chiplets with similar yields.[7–9,15,26] Both methods yield assemblies consisting of single components per receptor. Instead of applying a single die per receptor site, this report describes a self-tiling concept to cover domains of different size and shape with closely packed tiles that are much smaller than the domain size itself. The process to apply the tiles is driven by a stepwise reduction in interfacial free energy where the tiles are first collected and pre-oriented using an oil-water interface before they are introduced to a solder-patterned substrate that is pulled through the interface. Patterned transfer and packing occurs in a progressing linear front as the liquid recedes from the substrate, in a similar manner as previously reported,[27] but now results in the packing of microtiles in predetermined domains. The introduction rate typically exceeds 10 000 tiles per min and is limited by a number of factors, including the widths of the substrate/assembly vessel and the size of the tiles. The current system has a 1 cm^2 interfacial oil-water interface, which limits the amount of tiles per experiment at the interface to 250 000 when considering 20 μm^2 tiles and 40 000 when using 50 μm^2 tiles, for example. Additionally, in a container of a given size and width, the assembly process exhibits a higher introduction rate for smaller tiles: The rate scales inversely with the square of the tile size. In other words, a 10× size reduction of the tiles yields a 100-fold increase in the rate of introduction. The number of tiles that are introduced at the surface is generally larger than the number that assembles on the solder coated domains. Actual assembly rates depend primarily on the product of the tiles' introduction rate to the solid interface and the fraction of the solder coated domains' area (in units of integer tiles) covering the substrate. The observed assembly rates for 20 μm^2 tiles exceeded 10 000 tiles per min, which is a large number when compared to a state of the art serial robotic chip assembly machine, where 100 times smaller rates (a few components per second) are difficult to achieve. Moreover, the minimal component size, currently $(3\ \mu m)^2$, exceeds what is commonly possible in robotic assembly by a factor of 100. We also demonstrate the assembly of tiles on planar and curved surfaces over increasingly large domains. The largest domains contain over 6500 tiles, close-packed with less than 3% vacancies. As an application, we demonstrate the fabrication of a flexible, monocrystalline silicon solar cell on a polyethylene terephthalate (PET) substrate, which is covered with Si tiles that are 20 μm thin. The approach reduces the required usage of Si by a factor of 10 when compared to conventional 200 μm thick, rigid monocrystalline solar cells. The structure is then combined with an acrylic micro-concentrator lenticular array (Edmund Optics), achieving a total Si material reduction factor of ~22. The process distinguishes itself from prior self-assembly methods: it increases the area filling factor when compared to single chip-per-receptor assembly experiments where the spacing between components is typically larger than the component size. It also extends the minimal component size to the sub-100 micrometer scale, since it eliminates the dependency of gravity and sedimentation of prior methods,[5–9,15,20–26] which become increasingly ineffective to introduce highly scaled components to a substrate surface;

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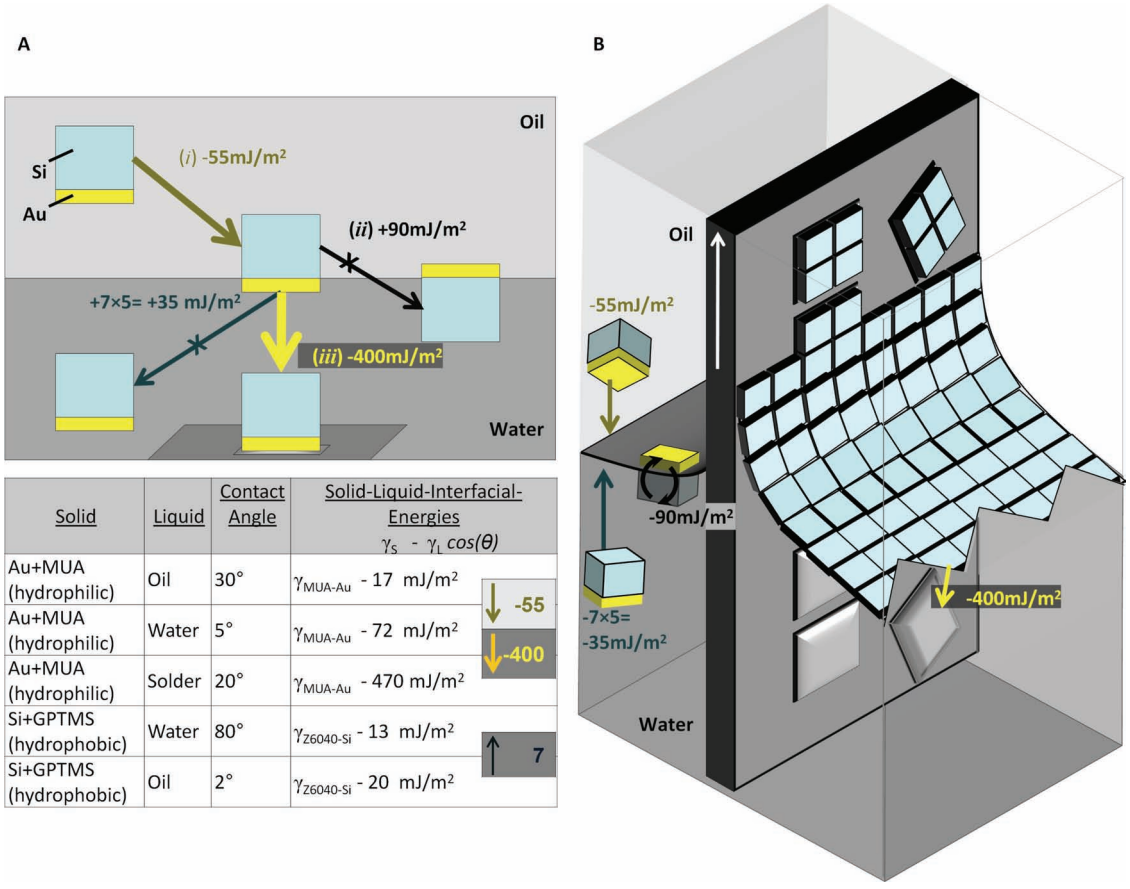

Solid	Liquid	Contact Angle	Solid-Liquid-Interfacial-Energies $\gamma_S - \gamma_L cos(\theta)$	
Au+MUA (hydrophilic)	Oil	30°	γ_{MUA-Au} - 17 mJ/m²	-55
Au+MUA (hydrophilic)	Water	5°	γ_{MUA-Au} - 72 mJ/m²	-400
Au+MUA (hydrophilic)	Solder	20°	γ_{MUA-Au} - 470 mJ/m²	
Si+GPTMS (hydrophobic)	Water	80°	$\gamma_{Z6040-Si}$ - 13 mJ/m²	7
Si+GPTMS (hydrophobic)	Oil	2°	$\gamma_{Z6040-Si}$ - 20 mJ/m²	

Figure 1. Transfer and self-tiling procedure of Si tiles at a liquid-liquid-solid interface employing an energy cascade (A) to (i) move tiles from a suspension to the interface (55 mJ/m^2), (ii) pre-orient the tiles within the interface to face in the right direction (90 mJ/m^2), and (iii) transfer the tiles to molten solder domains of different size and shape through dipping (400 mJ/m^2). The illustration depicts the situation for an oil water interface and tiles made out of Si (SU-8 is detailed in main body), which carry a Au contact on one face. Depicted Au and Si surfaces are treated using hydrophilic MUA and hydrophobic GPTMS functional groups and yield the tabulated measured contact angles, calculated solid-liquid-interfacial-energies, and energy differences (gray boxes to the right) required to drive the process. (B) The available area and curved shape of the interface cause the components to form a closely packed 2D raft. Upward motion of the substrate yields a dynamic contact angle where the receding water layer becomes sufficiently thin for the gold to contact the solder domain allowing the sections of the raft to transfer to the solder domain. Patterned transfer and self-assembly on molten solder is favored by 400 mJ/m^2 within this layer.

highly scaled components tend to stay suspended in solution while agitated. Component transport in this study is achieved using a liquid-liquid interface and is driven by a stepwise reduction of the interfacial free energy.

Figure 1 illustrates the experimental strategy of surface tension directed transfer and tiling of ultra small tiles at a liquid-liquid-solid interface. The process uses a stepwise reduction of the interfacial energy (Figure 1A) to (i) move Si-tiles from a suspension to the interface (55 mJ/m^2), (ii) pre-orient the tiles within the interface to face in the right direction (90 mJ/m^2), and (iii) transfer the rafted tiles to molten solder domains by dipping (400 mJ/m^2). To achieve this energy cascade, it is necessary to correctly choose and/or adjust the surface energies. We tested a water-oil interface and tiles made out of SU-8 and silicon (20 µm wide, 20 µm deep, 10 µm thick and 60 µm wide, 60 µm deep, 20 µm thick, respectively) with a gold-coated contact on one face. The gold surface was treated with a mercaptoundecanoic acid (MUA) self assembled monolayer (SAM) in a 10 mM (ethanol) solution for 15 min to render it hydrophilic, while the silicon faces were treated to become hydrophobic using 3-glycidoxypropyltrimethoxysilane (GPTMS, Dow Corning Z-6040) with 200 mM GPTMS in ethanol for 15 min. The SU-8 surface was hydrophobic and needed no adjustments. These treatments yield the measured and tabulated (Figure 1A, bottom) contact angles and interfacial energies, respectively, between the solids and liquids as determined using Young's equation $\gamma_{s,l} = \gamma_s - \gamma_l \cos(\theta_{s,l})$[28] where γ_s (unknown) is the surface energy of the solid, γ_l (known) is the surface energy of the liquid, and $\theta_{s,l}$ is the measured contact angle (known). The surface energy of water, silicon oil, and solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida) are 72, 20, ~500 mJ/m^2, respectively, at a temperature of 95 °C where the solder it molten. The surface energies of the solids γ_s (typically unknown) are not needed as this parameter cancels out when computing the energy differences. For example, considering the illustrated cubic component, the transition from the oil side to the interface is favored because the hydrophilic gold surface prefers to be in contact with water instead of oil;

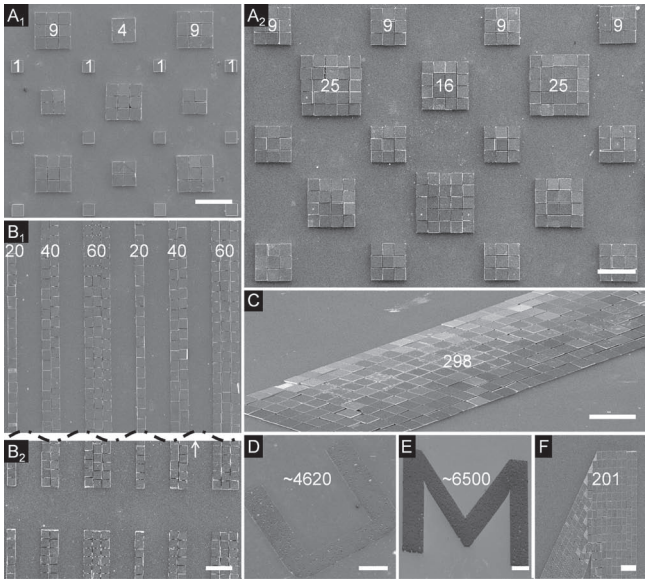

Figure 2. SEM images of tiled domains of different size. (A) Square domains with room for 1, 4, 9, 16 and 25 silicon tiles, 60 µm on a side. (B1) Center and (B2) end region of 5 mm long linear domains measuring 1, 2, and 3 component widths wide. (C) Rectangular domain with room for 300 Si-tiles. (D,E) Large letter shaped domains with room for thousands of 20 µm wide SU-8 tiles which cover >97% of the area. (F) Close-up view of a typical grain boundary in asymmetric elbow sections of letter shaped regions. Scale bars are 180 µm with the exception of large area domains (D,E) where 440 µm is used.

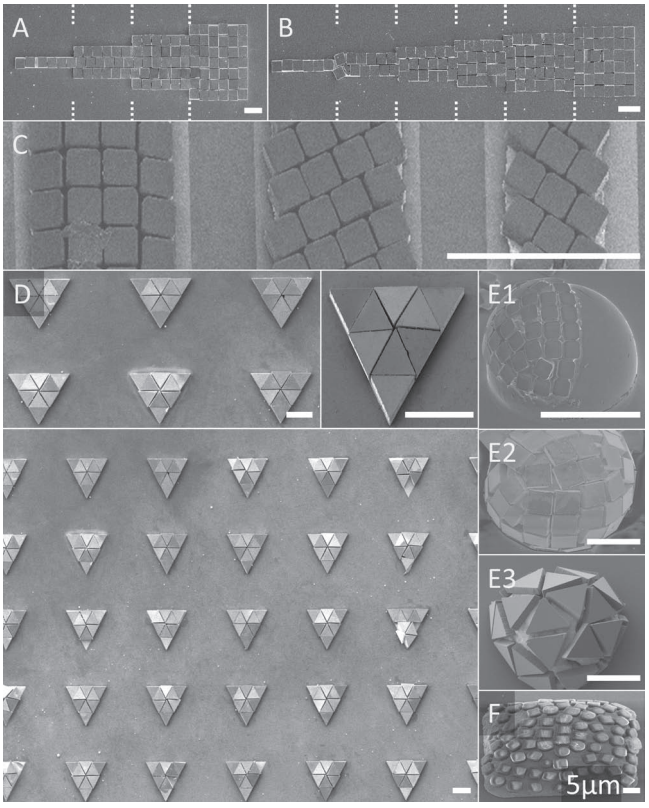

Figure 3. SEM images demonstrating self-tiling behavior and design rules. (A,B) SEM images of domains that allow (A, no defects) and hinder (B, one defect) lateral sliding/ annealing across the dotted lines; domain (B) does not support lateral sliding and one out of 126 tiles is misaligned. (C) Domains where the width is reduced from 4 to 3.5 to 2.5 violate the integer multiple widths requirement, which leads to new arrangements that maximize area coverage. (D) SEM images of triangular domains that are tiled with 270 triangular Si tiles showing one defect. (E) Spherical domains with at least 100 µm radius of curvature using tiles of (E1) 20 µm square SU-8, (E2) 60 µm square silicon, and (E3) 100 µm triangular Si. (F) 3 µm-sized ultra-small SU-8 tiles. 120 µm scale bars unless otherwise indicated.

transfer to the interface is favored by 55 mJ/m^2 = $\gamma_{Au,water} - \gamma_{Au,oil} = \gamma_{oil}\cos(\theta_{Au,oil}) - \gamma_{water}\cos(\theta_{Au,water})$. The components are confined to this interface since they face a 35mJ/m^2 = $(\gamma_{Si,oil} - \gamma_{Si,water})*5 = (\gamma_{water}\cos(\theta_{Si,water}) - \gamma_{oil}\cos(\theta_{Si,oil}))*5$ energy barrier preventing them from completely entering the water because the 5 hydrophobic Si sides prefer to remain in contact with oil instead of water. For a cube to be oriented upside down within the interface would require the sum of 90 mJ/m^2. Consequently the components are introduced to the solder with the correct orientation whereby the gold side faces the solder with a water layer in between. Solder has a higher affinity to wet the gold contact than water and attachment is favored by 400 mJ/m^2.

The actual transfer and self-assembly onto the substrate occurs as the sample is pulled upward through the interface (Figure 1B). Upward motion at a typical speed of 30 mm/s reduces the contact angle, forming a receding water layer that becomes sufficiently thin for the gold to contact the solder. Transfer of the tiles to the solder coated substrate occurs within this thin progressing interface, in a conveyor belt-like fashion. Analogous to the step-like growth observed during epitaxy, newly arriving tiles occupy the remaining space next to assembled tiles. For the assembly to work well, the following conditions were essential: The temperature has to be maintained constant, which is achieved using a heated ethylene glycol bath that is kept at 95 °C surrounding the glass assembly container. Metal surfaces including the solder must be free of surface oxide, which is maintained by reducing the pH of the assembly solution to pH 2.0 through the addition of hydrochloric acid. It is possible to get good (>90% coverage) in a single pass, however, full coverage (99%-100%) requires several passes through the interface. Assembly in this system occurs only during upward motion. Downward motion removes loose unassembled tiles, which transition back to the liquid-liquid interface. Saturation is observed in 5–10 passes, which takes less than 1 min. The short, <1 min, assembly time is an important advantage over previous settle assembly trials for reasons further detailed in the references section.[29]

Figure 2 depicts self-tiling results where the size of the receiving solder domains has been increased to make room for an increasing number of microscopic tiles. Defect-free tiling is possible at predetermined locations if the side length of the domain is an integer multiple of the tile size, as illustrated using domains with room for 1, 4, 9, 16, or 25 60 µm-wide silicon tiles (Figure 2A). Figure 2B shows an example of linear domains of various widths where perfect arrangement is possible over millimeter-long distances. Limits of the tiling process begin to appear when the individual domains have room for several hundred tiles. For example, the domain depicted in

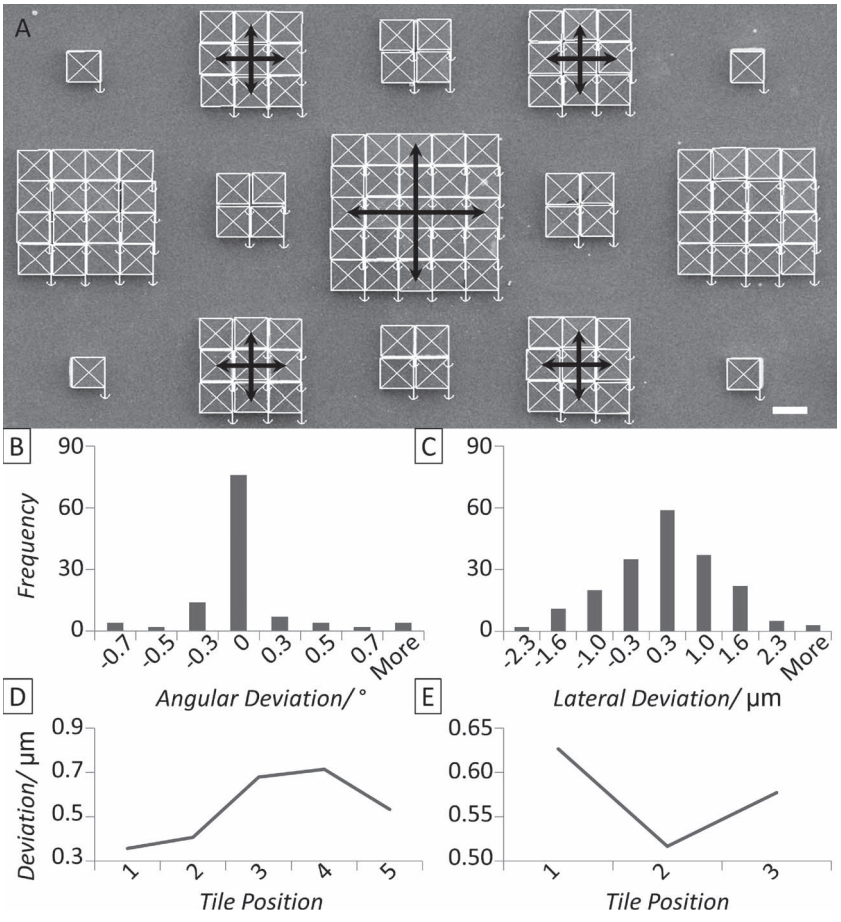

Figure 4. Measurement to determine the lateral and angular alignment precision. (A) SEM image overlaid with CAD measurement guides. (B) Histogram of the recorded angular deviations with a calculated STD of 0.3°. (C) Histogram of the lateral deviations with a calculated STD of 1.1 µm. (D) Lateral deviations of tiles along the highlighted center row and column of the 5 × 5 tile region showing improved accuracy at the region boundaries. (E) Lateral deviations of tiles along the highlighted center rows and columns of the depicted 3 × 3 tile regions wherein the center tiles have better alignment. 60 µm scale bar.

Figure 2C has room for 300 tiles but only 298 tiles assembled onto the surface. On increasingly large domains with room for many thousands of tiles, grain boundaries will finally emerge. The letters U and M in Figure 2D and Figure 2E provide examples where we used domains with a footprint that violate the crystallographic symmetry of the square shaped components. These domains have room for 4600–6500 microscopic SU-8 tiles (20 µm side length) and >97% of the area is covered with tiles. In these types of structures, most of the imperfections occur in rounded regions and in elbows where crystal fronts merge (Figure 2F). Single crystal domains with 200–500 tiles are commonly observed.

Figure 3 shows self-tiling images resulting from testing various domain and tile sizes and shapes. In Figure 3A, the width of the domain is adjusted to receive 1, 3, 5, and 7 rows of Si tiles, a design that maintains the array's periodicity (rows can slide from left to right), with defects tending to be less likely. The domain illustrated in Figure 3B violates this design rule. Here, the domain received 1, 2, 3, 4, 5, and 6 rows of Si tiles. The rows cannot slide from left to right and the lattice periodicity breaks down. A crystal boundary is forced to form at each transition and a slightly reduced ordering is observed due to the reduction in the extent of sliding motion that is allowed. Another design rule for the domains suggest the use of dimensions that are integer multiples of component lengths; violating this rule causes tiles to be arranged in a somewhat less predictable way to maximize coverage. Figure 3C illustrates this behavior for a solder domain where the width is decreased from 4 to 3.5 to 2.5 component widths, resulting in lattices of 20 µm wide SU-8 components with positive and negative slopes that cannot be predetermined. This process is not limited to specific tile and domain geometries and other regular polygons can be used as well. Figure 3D shows equilateral (100 µm side length) triangular silicon tiles tessellating an array of triangle domains wherein the individual domain size was chosen to provide room for 9 tiles. Assembly yields and area coverage in these types of assemblies exceed 99%. Figure 3E, meanwhile, tests an instance where the rules of matching tile and target domain geometry are violated. The depicted spheroids are ~200 µm in diameter silica beads with a receptor domain on top to receive (3E1) 20 µm square SU-8 blocks, (3E2) 60 µm square silicon tiles, and (3E3) 100 µm triangular silicon tiles. In these cases, the >99% coverage can no longer be sustained since the tiles are not optimized to match the surface. It should be noted that the process can be scaled to smaller and thinner components. Figure 3F depicts the results of the assembly of 3 µm-sized SU-8 parts that are 2 µm thick. The image shows a reduction in area coverage that can be explained by the larger variation in size. We believe that scaling can continue beyond the illustrated levels; the self-assembly of phospholipids into two dimensional sheets at an oil/water interface can be seen as an analogue that supports this belief. One challenge from a mechanical point of view, however, could be found in very thin, low aspect ratio tiles, which are mechanically less robust than those used in this study. While the handling of components using fluids might be less destructive than using mechanical tools, a backing layer would be required in these cases to add mechanical strength during the self-assembly process to avoid damage and folding. This layer may be as simple as a layer of resist that could be removed after the assembly.

Figure 4 provides a statistical analysis of the alignment accuracy of the given assemblies. We overlaid computer aided design measurement guides as shown in Figure 4A in order to take accurate location and angular deviation measurements on a variety of tiled regions. By first averaging the row and column X and Y values, we were able to calculate each tile's lateral deviation from the average. Figures 4B and 4C provide histograms of the recorded lateral and angular deviations across the image, which exhibit standard deviations of 0.3° and 1.1 µm, respectively. We also looked at the lateral deviation as a

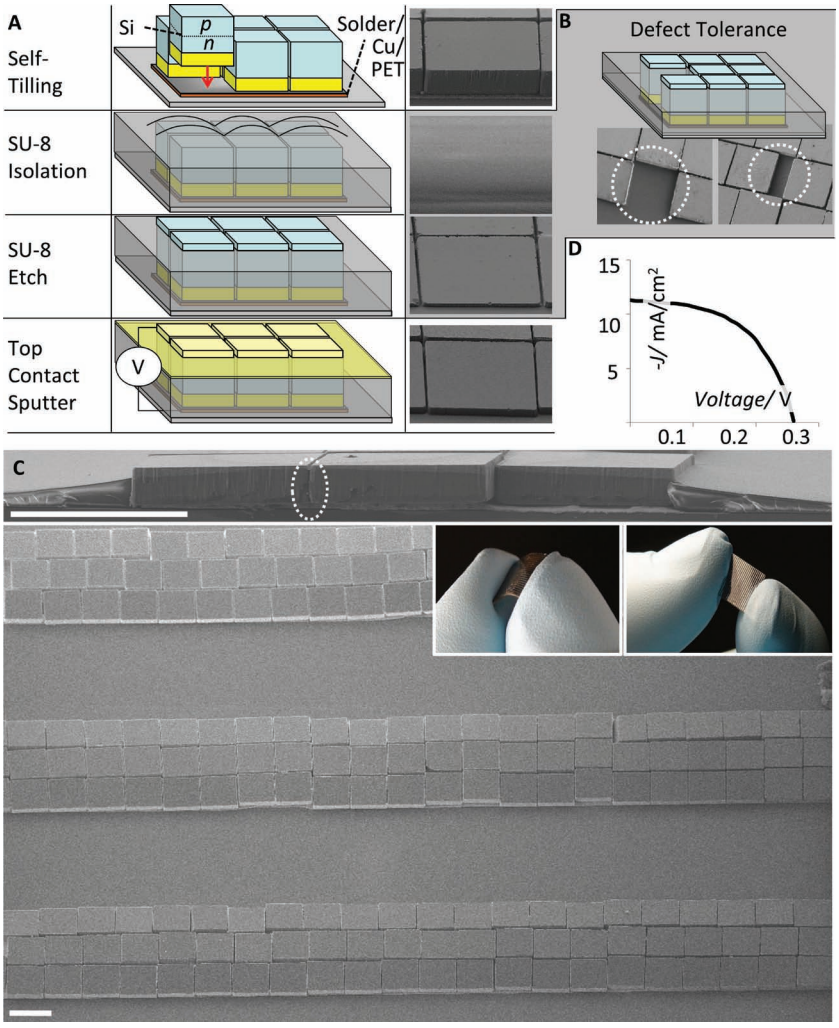

Figure 5. Flexible, segmented, self-tiled monocrystalline Si solar cell fabrication procedure, result, and characterization. (A) Assembly and isolation process with SEM images representative of each step. (B) Defect tolerant design strategy and sample micrograph illustrating how vacancies and lattice mismatches are filled in with SU-8, preventing short circuiting to the substrate. (C) Cross section, top view, and photographs of the device. (D) Resulting *I–V* curve. 60μm scale bars.

function of the position within tiled domains, since we noticed that the positional accuracy varies changes slightly with domain size. Figure 4D shows the average displacement along the row and column highlighted in the 5 × 5 tile region. Figure 4E shows a similar plot for the four 3 × 3 regions. As a general trend we observed that, for larger regions, the best positional accuracy will be observed at the edges of the pattern. The trend is reversed for very small domains where imperfections in the domain boundary are isolated and tend not to propagate to the inner components. Overall, these variances are small and the alignment accuracy that we observed is presently limited by the precision of the fabrication steps. The observed alignment accuracy using the etching techniques that we have used is commonly between 1–2% of the component size.

Figure 5 illustrates an application of the self-tiling process realizing a segmented monocrystalline solar cell on a flexible PET substrate while reducing the material use of Si by a factor of 10 when compared to conventional monocrystalline cell architectures. The material reduction is achieved by using 20 μm thin silicon tiles instead of commonly used 200 μm thick Si wafers where most of the Si is used to provide a mechanical support. The self-tiling process covers more than 98% of the solder coated areas and can be applied to the fabrication of thin flexible solar cells. The difference between the Si-tiles in this figure and the Si-tiles used in previous test experiments is that they carry a *p-n* junction, which is fabricated using a LPCVD-deposited phosphosilicate glass and a high temperature diffusion step before they are released from their source wafer and assembled onto the flexible PET substrate; the section on component fabrication provides further details. The process steps to form the solar cell modules shown in Figure 5A make use of a SU-8 isolation layer, which serves to electrically insulate the top and bottom electrodes to prevent short circuits. This layer is applied by spin coating before it is etched back in a reactive ion etcher to reveal only the p-doped region of the tiles, while protecting the n-doped region. The section on component fabrication provides further processing details. This architecture is further designed to be tolerant of tiling defects (Figure 5B) in such a way that the SU-8 fills in voids, locations of missing tiles (vacancies), lattice mismatches, and interstitial regions, ensuring that the modules' electrodes remain electrically isolated. Specifically, SU-8 and other polymers form a thinner film over protruding objects when compared to valleys when spun. This self-leveling behavior makes the cells tolerant against assembly defects; a missing Si tile, a lattice mismatch defect (highlighted regions, Figure 5B), or the interstitial regions (highlighted in cross section, Figure 5C) will not cause a short and failure of the cell module since these regions are coated with insulating SU-8. As a top contact we used a semitransparent 20 nm thin sputter deposited film of Au, however, materials including transparent conducting oxides (TCOs) could be used as well. Connecting the top contact to the conducting solder pad below completes the electric circuit. Figure 5D shows the resulting solar cell module *I–V* curve under 45 mW/cm^2 solar radiation, producing a fill factor of 0.54 and an efficiency of 4.18%, using a solar simulator (Philips PAR38 lamp, calibrated with an International Light Technologies 1400-A photometer). We tested the cells before and after assembly and found no measurable difference in their electrooptical properties after being exposed to the self-assembly procedure and oil-water interface. The 20 μm thin layer of Si adds little thickness to the 130 μm thick PET substrate and the cells retained the electrical properties when bent, as long as the radius of curvature remained above 1 cm, which is similar to previous results.[27] We have not tested the effects of fatigue and minimal possible radius

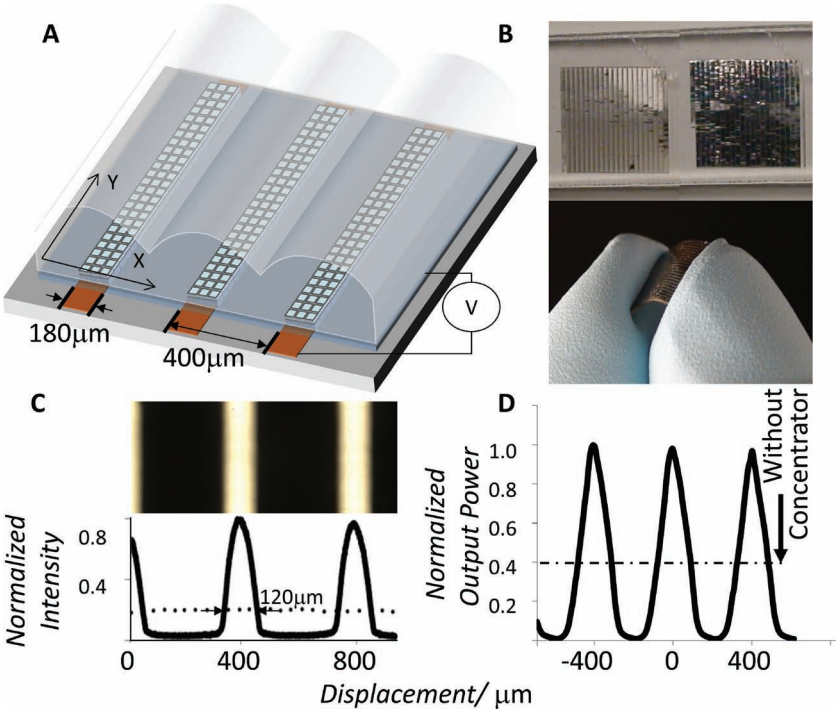

Figure 6. Photovoltaic Concentrator Module – schematic, result, and characterization. (A) Schematic showing lenticular concentrator array, tiled chiplets, and dimensions. (B) Optical images of the completed module with the applied concentrator array misaligned (left), aligned correctly (right), and removed. (C) Optical image and intensity profile of the concentrated light observed through a microscope. Dotted line represents no concentrator present. (D) Normalized power observed when the concentrator array is shifted in the *x* direction.

of curvature, but have observed situations where the top contact failed due to excessive bending.

Figure 6 details how the silicon tiles are used to form parallel 180 μm wide stripes of Si that are compatible with an acrylic lenticular array that is used to form a microconcentrator-enhanced solar cell sandwich structure. The lenticular array we used was fairly thick (~2.2 mm), which resulted in a final device structure that was no longer flexible. Specifically, we used a commercially available concentrator array (Edmund Optics, P/N NT43–028) that was placed on top of the solar cell module such that incident light was focused onto the parallel stripes of tiled Si (Figure 6A). The radius of curvature of the cylindrical microlenses is ~0.83 mm, corresponding to a focal length of ~2.2 mm. This particular lens array has an area concentration factor of ~4. In our experiments we used collimated light to yield an observed width of the focused lines of light (full-width passing 80% of the light) of ~120 μm (Figure 6C); the dotted line represents the intensity level without the lenticular array. Figure 6B shows optical photographs of the solar cell module underneath the concentrator array. The left image depicts the instance when the lens array is poorly aligned: The white paper underneath the structure becomes visible in this case. The dark specks represent excess tiles that have not been completely washed away. These tiles are not electrically connected. The image to the right shows the situation where the lens array is correctly aligned to funnel the light to the electrically connected tiles; the paper background is no longer visible and the structure appears dark. To test the efficacy of the microconcentrator, a micromanipulator was used to shift the lens array perpendicular to the tiled lines. The resulting normalized power plot is shown in Figure 6D where the dotted line provides the reference output power of the structure without the concentrator. For a constant illumination of 45 mW/cm^2 solar radiation the 4× concentrator array provided a ~2.5 fold increase in output power. The discrepancy can be explained by losses due to the added concentrator/interfaces and due to non-uniformities in the shape of the intensity profile. From a Si material reduction point of view the concentrator array in combination with the 20 μm thin silicon tiles reduces the amount of Si by a factor of 22 (20 μm thin, 180 μm wide Si strip on a 400 μm pitch) when compared to a conventional 200 μm thick, rigid monocrystalline Si solar cell modules.

We demonstrated a surface tension-directed tiling approach to assemble and electrically connect microscopic semiconducting tiles at predetermined locations on flexible supports. The liquid-liquid-solid interface proved to be a successful mechanism to deliver highly scaled silicon and SU-8 tiles to the substrate primarily since it eliminates the dependency on gravity and sedimentation of prior concepts that were limited to >100 μm sized parts. Minimal tile size (3 μm) and throughput (10^3–10^4 tiles/min) exceed prior high yield (>98%) component-to-substrate self-assembly methods. We anticipate that the method can be further improved through automation. The ability to define a triple interface and linear front where tiles arrive at the surface in a compacted pre-oriented fashion, much like in a Langmuir-Blodgett trough, provides a number of new opportunities to facilitate transfer of semiconducting materials to predefined regions on foreign substrates. "Roll-to-roll"-like system prototypes are possible extensions. Applications should not be limited to solar cells. Integration and distribution of microscopic light sources and energy producing elements are possible extensions.

Experimental Section

Passive SU-8 Tiles: A 500 μm p-type silicon wafer (Ultrasil, Hayward, CA) was coated with 13 nm Omnicoat (Microchem, Newton, MA). SU-8 2010 (MicroChem, Newton, MA) was spin-coated at 3000 rpm for 30 s and baked at 65 °C for one and 95 °C for 2 min. After a 132 mJ/cm^2 UV patterning, post-exposure bake (PEB) of 65 °C for 1 min and 95 °C for 2 min, the SU-8 was developed for 4 min. in propylene glycol methyl ether acetate (PGMEA). The Omnicoat was removed by a 40 s reactive ion etch (O2–100 sccm-100 W-100 mTorr), 200 Å of chromium and 3000 Å of gold were deposited by e-beam evaporation, and the Omnicoat was underetched by Microposit MF-319 developer (Shipley), releasing the components. These were rinsed in isopropyl alcohol and soaked in (10 mM) mercaptoundecanoic acid in ethanol for 15 min.

Si Solar Cell and Passive Tiles: The tiles were fabricated on a p-type silicon-on-insulator wafer (SOI, 20 μm device layer, 0.095–0.1 Ω/cm^2,

Ultrasil, Hayward, CA) that was given a standard clean: (1:1:5) $NH_4OH + H_2O_2 + H_2O$ at 80 °C, 15 min, (1:50) $HF + H_2O$ at 25 °C, 15 s, (1:1:6) $HCl + H_2O_2 + H_2O$ at 80°C, 15 min, and finally (1:50) $HF + H_2O$ at 25 °C, 15 s. The device layer of the solar cell tiles was doped n-type using a 3500 Å LPCVD-deposited phosphosilicate glass (PSG) layer as a source. The phosphorous diffused into the silicon in a nitrogen ambient at 1150 °C for 3 h. The remaining PSG was stripped in a BOE etch. The passive tiles did not undergo doping. Next, 200 Å of Cr and 2000 Å of Au were deposited by e-beam evaporation. These were patterned by exposed spin-coated photoresist (Microposit 1813, Shipley, Phoenix, Arizona). The Au surrounding the component pads was etched in GE-6 (1:10) (Acton Technologies, inc., Pittson, PA) for 9 min. and the chromium was etched in Cr-12S (1:4) (Cyantek, Corp, Fremont, CA) for 80 s. Finally, the silicon was etched using a deep reactive ion etcher. The buried oxide layer was etched in 49% HF for 7 min to release the completed silicon tiles. These were treated with (10 mM) mercaptoundecanoic acid (MUA) in ethanol for 15 min, rinsed in isopropyl alcohol, and soaked in (200 mM) glycidoxy functional methoxy silane, Dow Corning Z-6040, in ethanol for 15 min. Finally, they were baked at 115 °C for 5 min.

Solder domains on Si: A 500 µm thick p-type silicon wafer (Ultrasil, Hayward, CA) was patterned by liftoff. It was cleaned in sulfuric acid and hydrogen peroxide at 115 °C for 15 min before being rinsed and etched in HF (1:10). Photoresist (Microposit 1813, Shipley, Phoenix, Arizona) was spin-coated at 2500 RPM for 30 s. After a soft-bake at 105 °C for 1 min, the substrate was patterned with 96 mJ/cm^2 UV light and developed in (1:5) Microposit 351 + H_2O developer for 25 s. 200 Å Cr and 3000 Å Cu were then deposited by e-beam evaporation. Finally, acetone was used to perform liftoff and the pads were dip-coated with solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida).

Solder domains on flexible PET: A 130 µm thick propylene terepthalate (PET) sheet was cleaned in isopropyl alcohol for 10 min then treated in a 100 W reactive ion etch ammonia plasma for 30 min. Next, it was sputter-coated with 3000 Å Cu. Photoresist (Microposit 1813, Shipley, Phoenix, Arizona) was spin-coated and exposed with 96 mJ/cm^2 UV light. After a 25-second developing step in (1:5) MIF-315 + H_2O developer, the copper was etched with ferric chloride for 60 min. Finally, the solder (Y-LMA-117, mp. 47 °C, Small Parts, Miami Lakes, Florida) was applied to the Cu regions by dip-coating.

Self-Leveling Polymeric Isolation Process: Following self assembly, SU-8 2010 was spin-coated at 2500 RPM for 30 s and soft baked at 65 °C for 10 min. It was flood exposed with 200 mJ/cm^2 UV light, baked for 10 min at 65 °C, washed in PGMEA for 4 min, and etched back using a reactive ion etcher (CF_4:20 sccm, O_2: 80 sccm, 200 W, 100 mT).

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[29] To replace a silicon transistor that switches a current of a given magnitude with an organic pentacene transistor requires roughly [(ρ_{Pent}/ ρ_{Si})^3, typ. > 1000] more material occupying [(ρ_{Pent}/ ρ_{Si}), typ. > 100] more area. This estimate considers transistors with channel length l, width w, height h and resistivity ρ wereby the proportions are $l = n \times w = k \times h$. Considering Si and pentacene, the resistance becomes $R_{Si} = \rho_{si} \times l_{si}/ [(l_{si}/ n) \times (l_{si}/ k)]$ and $R_{Pent} = \rho_{Pent} \times l_{Pent}/ [(l_{Pent}/n) \times (l_{Pent}/ k)]$ To handle the same current requires the same resistance which means that $l_{Si}/ l_{Pent} = \rho_{Pent}/ \rho_{Si}$. The required volume and material for the same task increases increases with (ρ_{Pent}/ ρ_{Si}).