A Multi-Story Power Delivery Technique for 3D Integrated Circuits

Pulkit Jain, Tae-Hyoung Kim, John Keane, Chris H. Kim
Department of ECE, University of Minnesota, Minneapolis, MN 55455 *{ jainx104, thkim, jkeane, chriskim }@umn.edu*

ABSTRACT

Integrating circuits in the vertical direction can alleviate interconnect related problems and enable heterogeneous chips to be stacked in a single package with a small form factor. This paper addresses the power delivery issues in 3D chips revealing some interesting facts and design challenges. A multi-story power delivery technique that can reduce the worst case DC noise by 45% and lower the overhead power consumed in the power supply network by 65% is proposed. A test chip layout in an SOI process, showing a 5.3% area overhead, demonstrates the feasibility of the scheme.

Categories and Subject Descriptors: B.7.1 [**Hardware**]: Integrated Circuits – *Types and Design Styles*

General Terms: Design, Performance

Keywords: 3D chip, power delivery, power supply noise, multi-story

1. INTRODUCTION

3D integration is recognized as a breakthrough technology for improving interconnect performance and reducing chip form factors [1][2]. Memory bandwidth, which has become a critical performance limiter in modern microprocessors, can be significantly increased by vertically stacking caches on top of processing cores. Extremely high memory densities have been demonstrated for stand-alone applications where multiple 2D memory chips are stacked in a single package. 3D integration technology also makes it possible to vertically integrate chips built in heterogeneous processes (e.g. logic, DRAM, flash, SiGe, InP) with slight additional cost compared to integrating monolithic chips. Recent advancements in Through Silicon Via (TSV) technology have transformed 3D integration from a laboratory exercise to a practical technology. Dimensions of state-of-the-art TSVs have shrunk below 1 micrometer which reduces the area and performance overhead for the electrical interconnection between the different tiers [2]. Here, the term "tier" is referred to each layer of devices and metal wires which are stacked to compose a 3D IC.

The premise of 3D integrated circuits has spurred research activity at virtually all levels of the 3D design hierarchy. The material and process community has recently made great strides in developing high yield and low cost TSVs with dimensions comparable to small logic gates [3][4]. The capability to improve TSV characteristics as traditional scaling continues makes 3D chips even more viable in future process generations. A host of techniques to deal with 3D chip design issues have been introduced by the circuit design and automation community. Thermal management is one of the most important design issues in 3D chips, as they have higher power dissipation per area and increased thermal resistance between the tiers due to the isolation layer. It is widely accepted that the processing cores, which generate the greatest amount of heat, should reside on the tier closest to the cooling device while circuits such as memory and analog/RF with relatively low thermal profiles should reside on the layers closer to the electrical interface. Various 3D architectures and interconnect models have been proposed to estimate the performance benefits, power reduction and die temperature [1][5]. Thermal aware placement and routing algorithms for 3D ICs have been presented in a number of prior publications [6][7][8][9]. Contactless signaling between the stacked tiers using the capacitive or inductive coupling principle has been gaining traction in the circuit design community [10][11][12]. That work is based on the premise that by utilizing the close proximity of the circuits, TSVs between the tiers for data signals can be eliminated, which may resolve wafer alignment issues and lead to lower process complexities. At the architecture and system level, benchmark programs were used to predict the memory bandwidth improvement in various 3D architectures [13].

Despite the recent surge in 3D IC research, there has been virtually no work from the circuit design and automation community on power delivery issues for 3D ICs. On-chip power supply noise has worsened in modern systems because scaling of the Power Supply Network (PSN) impedance has not kept up with the increase in device density and operating current due to the limited wire resources and constant RC per wire length [14]. This situation is worsened in 3D ICs as TSVs contribute additional resistance to the supply network and the number of pins for power delivery is fundamentally limited by the footprint of the 3D chip. For example, a 3D chip with n tiers can only have $1/n$ the number of power supply pins compared to its 2D counterpart which results in an n fold increase in the resistive and inductive parasitics. The increased IR and Ldi/dt supply noise in 3D chips may cause a larger variation in operating speed leading to more timing violations. The supply noise overshoot due to inductive parasitics may aggravate reliability issues such as oxide breakdown, Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). Consequently, on-chip power delivery will be a critical challenge for 3D ICs. This is contrary to the common perception where power delivery in 3D chips was considered no different than that in conventional 2D chips.

In this work, we specifically address the power delivery issues in 3D ICs. The highlights of this work are as follows:

- Compared to their 2D counterparts, we find that 3D designs have a much larger DC noise due to the added TSV resistance. The peak impedance at the resonant frequency is similar to 2D as the increase in inductive impedance is partially compensated by the increased damping from the TSV resistances.
- Low frequency supply noise is worst in the tier farthest to the supply pins (i.e. the bottom tier) while the high frequency noise is worst for the tier closest to the supply pins (i.e. the top tier).
- A multi-story power delivery technique is proposed for 3D chips. In this scheme, an external voltage source of $2V_{dd}$ or $3V_{dd}$ (or more) is applied, and power is distributed differentially between a (kV_{dd}) rail and a ((k-1)V_{dd}) rail using level conversions as required [15][16]. By recycling current between different power supply domains, the IR noise can be reduced by up to 45%.
- Design trade-offs between the number of stacked supplies, leakage power and via allocation has been analyzed in detail for the proposed multi-story power delivery scheme.

A 3D test chip layout in MIT Lincoln Lab's 0.18µm process showcases the feasibility of the proposed scheme. The PSNs in

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each tier are readily separated requiring only slight modification, which makes the scheme particularly attractive for 3D chips.

The organization of the paper is following. In Section 2, we reveal some important perspectives on power supply noise in 3D chips based on actual TSV parameters from a production level 3D process. In section 3, we give analysis results to propose a multi-story power delivery technique to mitigate the DC noise problem in 3D chips. Section 4 gives a chip layout implementation of the proposed scheme. Finally, section 5 draws a conclusion. This work uses MIT Lincoln Lab's 1.5V, 0.18µm 3D Fully-Depleted Silicon-On-Insulator (FD-SOI) process which has 3 tiers [4].

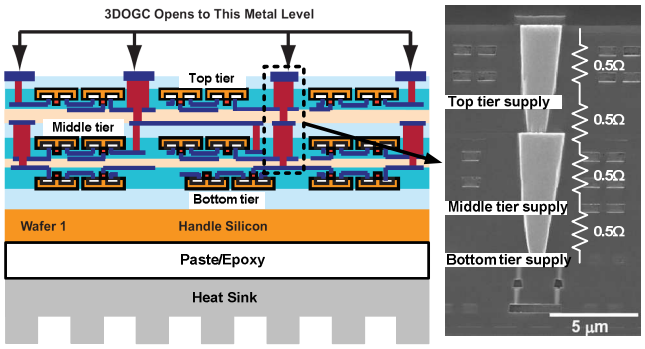
2. POWER SUPPLY NOISE: 2D VS. 3D

2.1 Introduction to 3D FD-SOI Process

Fig. 1(a) depicts the MIT Lincoln Lab's 3D FD-SOI process. This process has three tiers. The bonding pads are on the top tier, while the heat sink is typically below the bottom tier. Processors or other power intensive circuits would ideally be placed on the bottom tier in close proximity with the heat sink.

The tiers are interconnected through TSVs for electrical and thermal conduction. Fig. 1(b) shows the cross-sectional SEM photograph [4] of a stacked TSV connecting the back metal of the top tier with the top level metal of the bottom tier. A simplified resistance model is superimposed. Based on actual parameter extraction [4], each cone-shaped TSV has a resistance of 1Ω in this process and the stacked TSV, a total resistance of 2Ω. The top and middle tiers are aligned face-to-back, while the middle and bottom tiers, face-to-face, making the path from the top to middle tier longer and more resistive. We model this configuration by breaking up the total 2Ω stacked via-resistance into chunks of 0.5Ω, 1Ω and 0.5Ω as shown in Fig. 1(b).

The TSV resistance encountered in the supply path imposes new challenges in 3D power delivery vis-à-vis the conventional 2D case. First, the lower tiers experience worsened power supply noise due to the increased resistance in the power network. Furthermore, power intensive circuits have to be placed at bottom tier, which makes reliable power delivery even more difficult.



(a) (b)

Fig. 1 (a) Cross section of 3D FD-SOI process. (b) Simplified via resistance model aligned with a cross-sectional SEM.

2.2 Frequency Response of Power Network: 2D vs. 3D

The supply noise behavior in 2D circuits is fairly well understood [14]. However, in 3D, due to the TSV resistance in the power network structure, the supply noise characteristics in each tier should be revisited.. Fig. 2 gives the circuit models developed to compare the two cases. The resistance in 3D supply path would be dominated by the TSVs, ten of which are modeled here. There are a few assumptions made. First, the overall chip capacitance (3nF in typical 2D case) is split equally between the three 3D tiers. Second, due to the reduced footprint of the 3D die, the number of power pins would be third of the 2D case, leading to 3X increase in package parasitic inductance and resistance.

Since, noise at the bottom tier is predictably worst, we compare this tier's impedance response with the 2D case.

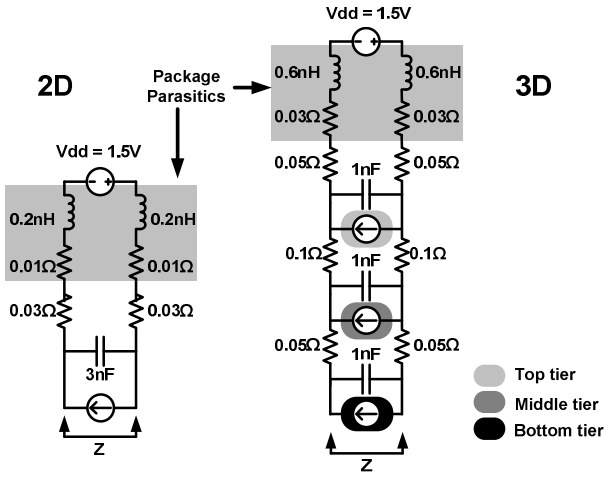


Fig. 2 Simplified PSN models for comparing impedance response in 2D and 3D.

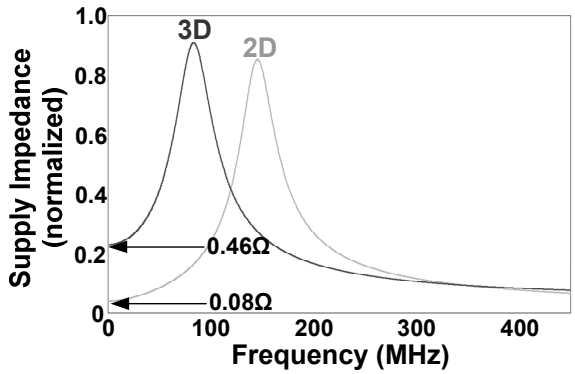


Fig. 3 Impedance response comparison between 2D and 3D.

The normalized impedance comparison is shown in Fig. 3, which illustrates the following:

- Low frequency impedance: The capacitors and inductors are open and short circuited, respectively. Therefore, the 2D model has an impedance of 2(0.01+0.03)=0.08Ω, while the 3D model has an impedance of 2(0.03+0.05+0.1+0.05)=0.46Ω. This indicates that for the same amount of current, the 3D chip will have 0.46/0.08=5.75X more IR drop compared to 2D.
- Resonant peak impedance: The resonant peak is determined by amount of damping and the value of inductance. Here, the increased inductance in 3D (due to the smaller footprint) is counteracted by the increased damping provided by the larger resistance drop to the bottom tier. Thus, the peaks show comparable values.
- Resonant frequencies: 2D circuits typically have a resonant frequency of around 50-300MHz, given by $f_{res} = 1/(2\pi\sqrt{LC})$. If the equivalent capacitance in 3D is same as in our model, due to the increased L, the peak is shifted to a lower frequency
- High frequency impedance: 2D and 3D impedances become comparable, and this is attributed to the shielding effect of the bottom tier capacitance – which is due to the fact that the capacitance becomes virtually a short at high frequencies. Thus, we can conclude that the *DC supply noise becomes a greater concern in 3D designs* as compared to its 2D counterpart.

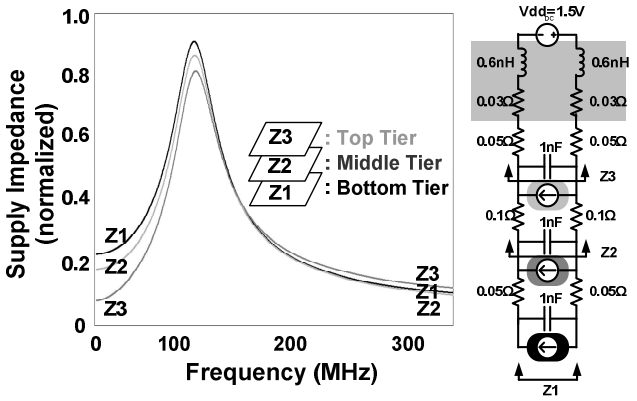


Fig. 4 Impedance response of the three tiers in a 3D IC.

2.3 Impedance Response of Power Supply in Each 3D IC Tier

To understand the supply noise behavior at different tiers, we simulate the AC impedance in Fig. 4 using the test circuit shown. The key results are as follows:

- Low frequency impedance: As expected, the DC and low frequency impedances, which are governed by the TSV resistances, show a worsening trend for the lower level tiers.
- High frequency impedance: The top tier has the largest impedance while the middle tier has the minimum AC impedance, which seems to be counter-intuitive. This characteristic is due to the shielding effect of the adjacent tier capacitances, which causes the effective damping resistances to be the largest for middle tier and smallest for the top tier. The above trend is more noticeable at high frequencies beyond the resonance peak.
- Resonant behavior: Since the shielding effect mentioned above is not significant at mid-frequencies, the resonance peak follows the lower frequency trend with bottom tier being the worst case. However, there is a reduced noise offset as noted from the simulated curves. Also, since the effective capacitance is the same for all tiers, the resonant frequencies are almost identical.

In summary, the AC impedance is worst for the bottom tier up until the resonant frequency, while beyond this point, the top tier has a slightly larger impedance value. Since the bottom tier is likely to contain circuit blocks with large current consumption due to thermal issues, the supply noise in the bottom tier (i.e. product of current and impedance) will become a major concern for 3D implementations.

3. MULTI-STORY POWER DELIVERY FOR 3D CHIPS

We have emphasized the supply noise problem in 3D IC architectures arising due to the large resistances associated with the supply path to the bottom tier. The problem is further difficult, since it is impractical to increase the TSV count due to the ensuing area overhead. In this section, we have extended the idea of a multi-story power delivery [15][16] to propose various architectures for suppressing power supply noise in a 3D IC.

Fig. 5 explains the basic concept of multi-story power delivery. The conventional supply network is modeled in Fig. 5 (a), where all circuits draw current from a single power source. Fig. 5 (b) shows the multi-story supply network with sub-circuits operating between two supply stories. (Note that here; "story" is only an abstraction to illustrate the nature of the power delivery scheme, as opposed to the 3D IC architecture, where circuits are physically stacked on top of each other.) In this scheme, current consumed in the "$2V_{dd}$-V_{dd} story" is subsequently recycled in the "V_{dd}-Gnd story". Due to this internal recycling, half as much current is drawn compared to the conventional scheme, with almost the same total power consumption. A reduced current is beneficial since it cuts down the supply noise. Thus, in the best case, if the currents in the two sub-circuits are completely balanced, the middle supply path will sink zero current. This results in minimal noise on that rail, as also illustrated in Fig 5.

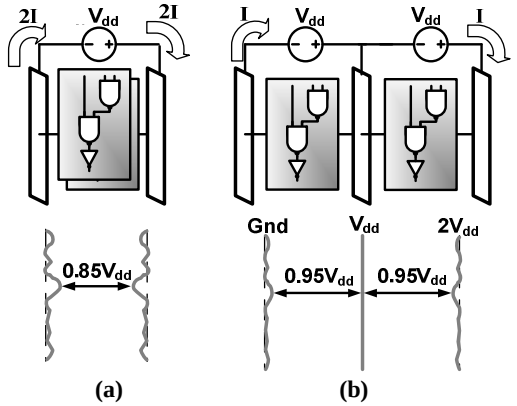


Fig. 5 Conventional and multi-story power delivery schemes [15][16]..

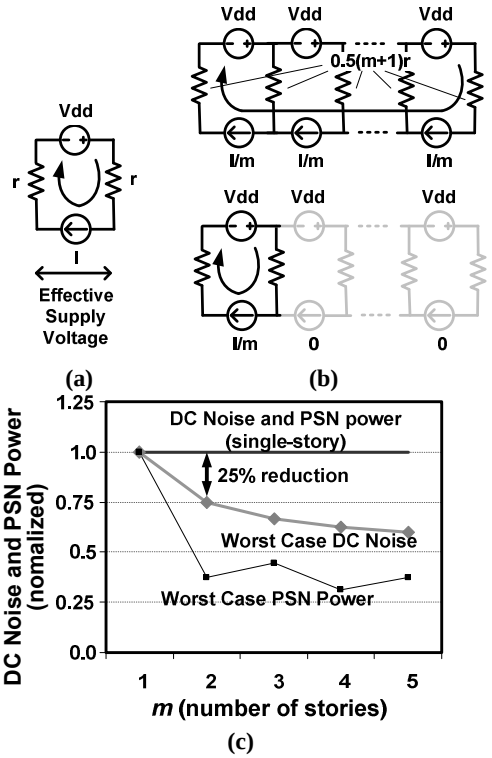


Fig. 6. (a) Conventional one-story PSN model. (b) Best case and worst case noise conditions in an *m*-story PSN. (c) DC noise and power consumption versus *m*.

3.1 Optimal Number of "Stories" in 3D ICs

We now consider a more generalized *m*-story power delivery scheme for 3D ICs. Fig. 6(a) gives a model of the traditional one-story supply structure, where we merge all tiers of a 3D IC into a single current source for simplicity. The resistance, *r*, would be the vertical path resistance contributed by the TSVs and is inversely proportional to their number. The total switching current of the 3D chip is denoted by *I*. With this model, we

calculate the worst case DC noise and power dissipation in the PSN as $2 \cdot I \cdot r$ and $2 \cdot I^2 \cdot r$, respectively.

Fig. 6(b) shows the proposed equivalent model employing *m*-stories. The net current is distributed in *m* equal *I/m* current blocks. Due to the increased number of supply paths, the overall effectiveness of this scheme should be judged with a constraint on area, equivalent to the TSV count. Thus, the total TSV number here (and in all the subsequent analysis) is assumed to be fixed at 2N. Therefore, each path in Fig. 6(b) has $2N/(m+1)$ TSVs, which translates to $0.5(m+1)r$, as the corresponding path resistance.

Some analysis results from the above proposed topology are useful in subsequent sections and we summarize them below.

- In the best case, if all stories are 'on', the middle supply paths have ideally no currents flowing, thus minimizing the supply noise for those tiers.
- Unlike the conventional scheme in Fig. 6(a), the worst case condition for noise occurs when only one story is on, while others are off as depicted in Fig. 6(b) (gray). The worst case noise comes out to be $I \cdot R \cdot (1+1/m)$.
- The maximum power consumption occurs when every alternate story is off. However, in the two story case, it would be the same as the case when both stories are on.

Fig. 6(c) shows the plot of the worst case DC noise and PSN power versus number of stories *m*. Clearly, the curve shows great returns in terms of power and noise for *m*=2, beyond which the returns diminish. Considering the overhead for partitioning the circuit and generating multiple power supplies, a two-story network is suited for our case.

3.2 Beneficial Effect of Leakage on PSN Supply

We now examine the two story PSN structures in Fig. 7, while considering leakage current in the off-stories assuming it to be $\alpha \cdot I/2$. In the present technology a leakage current of 25-50% of the on-current is a fair estimate. It is evident from Fig. 7(right) that the leakage current opposes the regular current flow and reduces the worst case drop across the common supply path. As calculated below the figure, compared to the single-story scheme of Fig. 6(a), we get a DC supply noise reduction of 44% and the worst case PSN power decrease of 62.5%, assuming an α of 0.5.

Next, we will employ the multi-story power delivery scheme to propose some 3D IC models.

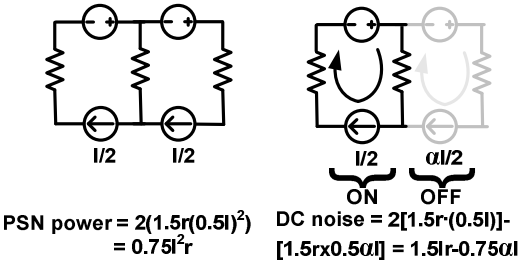


Fig. 7 Two-story PSN (left). Worst case for DC noise (right). α is the percentage leakage power.

3.3 Multi-Story PSN for a Memory-Memory-Processor Architecture

Fig. 8 shows the 3D PSN model of a memory-memory-processor architecture. The processor resides at the bottom tier, and is assumed to consume twice the memory tier current. The TSV count is 2N as before and the parasitic L and C components have been ignored for DC analysis. The equations for the worst case power dissipation in the supply nets and the worst case DC noise are depicted alongside the figure.

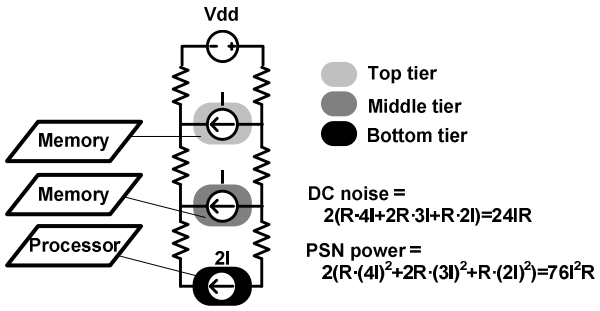


Fig. 8 PSN model of memory-memory-processor architecture in a single-story 3D IC design.

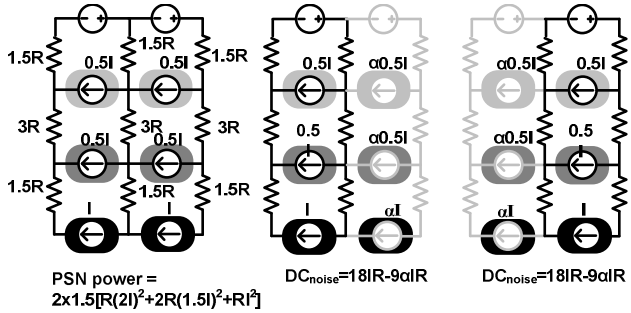


Fig. 9 Balanced multi-story power delivery for the 3D IC model. (a) All circuits switching representing worst case PSN power. (b) Left story switching (c) Right story switching.

Using the multi-story scheme, we propose an alternate 3D topology in Fig. 9(a), which we call the *balanced multi-story power delivery 3D IC model*. Here, each tier is split up into two equal sub-blocks with different supply stories The 2N vias are equally distributed in the three supply paths resulting in a 3/2X increased per path resistance. Fig. 9(b) and (c) show the two worst case possibilities, with the faded figure showing the off part conducing only leakage current. Thus at 50% leakage (α=0.5), we get a 44% reduction in DC supply noise, while a 62.5% decrease in PSN power calculated from the resistive dissipation in Fig. 9(a). The base case for comparison is the topology in Fig. 8. Note that these results are identical to ones from Fig.7. The advantage of this topology is the inherent balance in the two worst case scenarios, which if skewed degrades the DC noise as seen next.

The presence of multiple supply rails in the balanced multi-story scheme can lead to certain implementation issues, as discussed in section 4. A *coarse multi-story power delivery* model of Fig. 10(a), with single-storied tiers, is an alternate scheme, where the processor in the bottom tier is implemented in a different story from the memory tiers at the top. By doing so, the supply network in each tier can be left intact, simplifying the implementation. The worst case for PSN power, represented by Fig. 10(a), yields a value of $42 \cdot I^2 \cdot R$, a reduction of 45%.compared to the base single story case. By analyzing the two cases in Fig. 10(b) and (c), separately for IR drop we find the worst case noise is given by:

$$DC_{noise} = \max[(24IR - 6\alpha IR), (12IR - 12\alpha IR)]$$

where α is again the percentage of leakage current. At 0% leakage, this equals $24 \cdot I \cdot R$, which shows no improvement from the single-story case. At higher leakage currents, the effectiveness is better than the balanced model but is still limited by the skew of the DC noise in the two worst case possibilities, as seen from above

equation. This reveals further scope for improvement by redistributing the TSVs for different supply paths to optimize the overall worst case.

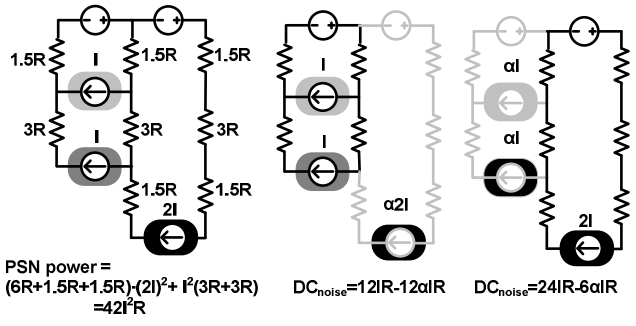


Fig. 10 (a) Coarse Multi-Story Power Delivery (b) Left story switching c) Right-story switching (worst case DC noise)

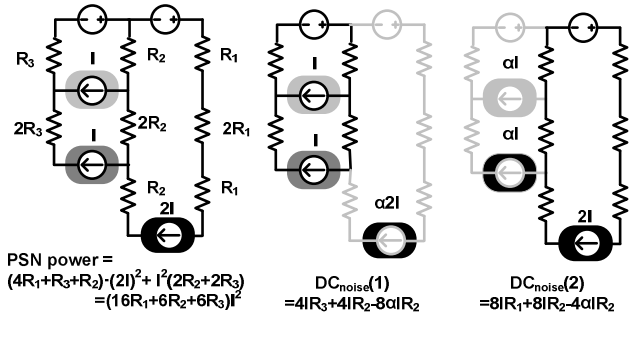


Fig. 11 (a) Non-uniform TSV distribution (b) Left Story Switching c) Right Story Switching

Table 1: DC noise optimization criterion at different leakage.

% leakage	Via Distribution (N_1, N_2, N_3)	DC_{noise} reduction	R_1,R_2,R_3 values
0%	0.86N, 0.86N, 0.28N	22.5%	1.16R, 1.16R, 3.5R
25%	0.95N, 0.79N, 0.27N	28%	R, 1.27R, 3.7R R
50%	N, 0.75N, 0.25N	34%	R, 1.33R, 4R

Fig. 11(a) shows the same circuit with a non-uniform via distribution, using the variables R_1, R_2 and R_3 which are not necessarily equal. The worst case for PSN power is Fig. 11(a). The two extreme cases with the worst case DC_{noise} are depicted in Fig. 11(b) and 11(c). Thus, we formulate *the optimal via distribution condition for minimal DC noise as a choice of R_1, R_2 and R_3 for which Max ($DC_{noise}(1)$, $DC_{noise}(2)$) is minimized with the fixed TSV constraint:*

$$N_1 + N_2 + N_3 = 2N \quad or \quad \frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}=\frac{2}{R}$$

Intuitively, the optimization should converge towards making the two worst cases equal. The DC noise results are presented in Table 1 for different α values. Thus, the proposed optimized scheme offers a 22-34% improvement in DC noise. Simultaneously, it would decrease the PSN power by as much as 37% (for α=0.5).

It should be noted that the above optimization was done to decrease the IR drop. Another criterion could be to minimize the PSN power expression shown in Fig. 11(a). Hence, we reformulate the *TSV optimization criterion for minimizing the power supply network as a choice of N_1, N_2, N_3 (or R_1, R_2, R_3) for which $F=16/N_1+6/N_2+6/N_3$ is minimized with the constraint that $N_1+N_2+N_3=2N$.* We substitute $N_1=2N-N_2-N_3$ into the expression for F, take partial derivatives with respect to N_2 and N_3 and equate to zero. We obtain $N_1=0.89N$ ($R_1=1.12R$) and $N_2=N_3=0.55N$ ($R_2=R_3=1.8R$). This yields an improvement in PSN power efficiency by 48% but degrades the supply noise.

It is important to emphasize that the balanced topology of Fig. 9 is preferable against the coarse topology of Fig. 11 for the memory-memory-processor architecture being considered here. The latter topology tries to balance the processor current with the memory current in the upper tiers. This may not yield significant noise benefit in the case when the processor current is much larger than memory current, making the two worst conditions for DC noise too skewed to seek any advantage from via optimization. However, the situation is different in the uniform memory-memory-memory scenario, as discussed below.

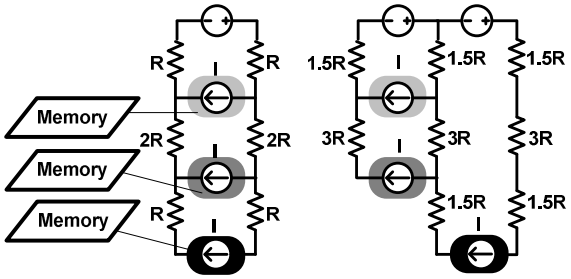


Fig. 12 (a) Memory-memory-memory in a conventional single-story design. (b) Proposed multi-story scheme.

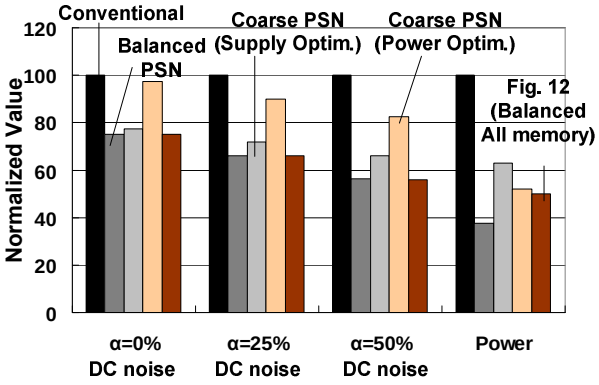


Fig. 13 DC noise and PSN power of different schemes.

3.4 Multi-Story PSN for a Memory-Memory-Memory Architecture

Unlike the topologies considered in previous discussion, the 3D IC model in Fig. 12(a) has monolithic memories on each tier having similar current drives. Fig. 12(b) is the preferred scheme in this case. The implementation is easy, since the different tiers can be readily separated as independent memory sub-blocks with different supply stories. The analysis follows that of the topology in Fig. 10, except that in this case the two worst cases are inherently balanced by the recycling of tier 1 current into tier 2 and tier 3, and no further optimization is required for noise. With α=0.5, this scheme offers a 44% and 50% reduction in noise and PSN power, respectively.

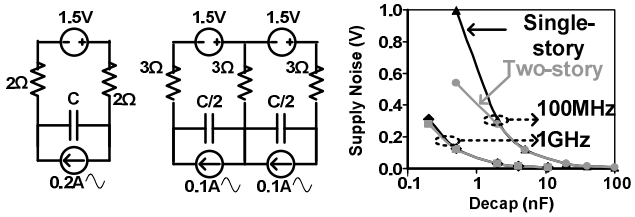
3.5 Comparison of Power Delivery Schemes

Fig. 13 summarizes the effectiveness of the various schemes, discussed in this section, in terms of PSN power reduction, and DC noise reduction at α=0%, 25%, 50%. As depicted, the multi-story technique proposed for 3D ICs has the potential to reduce the DC noise by 25%-45% depending on the preferred topology

and leakage power percentage. Also, PSN power can be simultaneously cut down by 37%-63%.

3.6 AC Supply Noise Characteristics

It is also important to gauge the immunity of the proposed scheme against AC noise. Figs. 14(a) and (b) show the test structures for comparison of AC supply noise at the bottom tier for the single- and multi-story schemes. The other tiers have been ignored for simplicity. In order to make the comparison fair, the same amount of decoupling capacitance (decap) is employed in both circuits, and the number of TSVs is assumed to be identical. In these simulations, the amplitude of the sinusoidal noise was set at 0.2A, and the supply noise was measured while varying the total amount of decap for both circuits equally. Global resonance is assumed to be typically around 100MHz, the reason for the chosen frequencies. Fig. 14(c) shows that the proposed circuit results in greater AC noise reduction with lower total amounts of decap, and a comparable performance with larger, more realistic decap values.



(a) **(b)** **(c)**

Fig. 14 (a) AC noise analysis setup for single-story supply. (b) AC noise analysis setup for multi-story supply. (c) AC noise comparison at 100MHz and 1GHz.

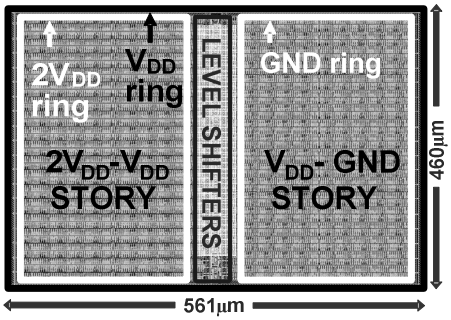


Fig. 15 3D chip layout of the multi-story power delivery scheme. TSVs are located along the supply rails on the periphery. The lower tiers are stacked below the shown view.

4. CHIP LAYOUT IMPLEMENTATION

To demonstrate the feasibility of the proposed scheme, we implemented a test layout of a 3D IC, shown in Fig. 15, using the MITLL-0.18µm FD-SOI design kit. Only the top tier is visible in the figure. Each tier is split up into two stories and powered by appropriate supply rails (highlighted in figure for visibility) that are laid as concentric rings. The TSVs are densely placed on these rails. In order for the stories to communicate with each other, level shifting logic was employed [15][16]. Due to the additional level shifters and supply path, there is a 5.3% area overhead over the conventional 3D IC design for the 516x460µm^2 test layout. Since, this was a SOI process where the transistor bodies are isolated; the balanced multi-story scheme in Fig. 9 was suited for implementation. However, in a bulk process, as NMOS devices on each tier have to share the same body bias, the coarse multi-story scheme of Fig. 11 should be employed.

5. CONCLUSIONS

This paper analyzes on-chip power delivery issues for 3D ICs using simple circuit models from MIT Lincoln Lab's 1.5V, 0.18µm 3D FD-SOI process. DC, rather than AC, noise is shown to become a greater issue especially in the bottom tier for a 3D IC. A multi-story 3D power delivery scheme that addresses this issue without incurring any area overhead has been developed and extended to curb supply noise in memory-memory-processor and all-memory 3D architectures. Simple DC analysis estimates a DC noise reduction of 25%-45% depending on the preferred topology and percentage of leakage power. In addition, PSN power is predicted to be cut down by 37-63%. The feasibility of the scheme is demonstrated using a 3D chip layout in an SOI process showing a 5.3% area overhead.

6. ACKNOWLEGDEMENTS

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